APPLICATION NOTE

System Application of SAB 9076/77 PiP Processor

AN96081

Philips
Semiconductors

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Abstract

Picture-in-Picture Controller SAB 9076 with colour decoders TDA 8315, TDA8310A and video processor TDA 4780.

This application note describes the possible configurations of the PiP-Controller environment, a rough description of the PiP-controller itself, the IIC-Bus registers and their controlling, a stand-alone evaluation boardset and gives some application advice.

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

System Application of SAB 9076/77 PiP Processor

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Summary

This application note describes some concepts to built in a PiP function in environments like TV-sets, Video recorders or satellite receivers. The proposals for implementing such a PiP application are shown and discussed in the chapter 2. Several conceptional aspects are taken into account.
The PiP controller itself is roughly described in chapter 3. For more detailed informations please refer to the application notes [5] and [6].
The major part of this application note, chapter 4, explains the PiP evaluation boardset in detail. The used IC's TDA 8315T, TDA 8310A and TDA 4780 are shown and explained in detail if necessary.The schematics are discusses in detail and application hints are given, too.
Because of the PiP evaluation boardset is designed as a modular system, the interfaces between the modules are described signal by signal with their characteristics. The layouts of the modules are attached.

I hope the user of our PiP evaluation boardset and this application note finds all the informations he wishes to know.

Special thanks I like to give to my colleagues in Nijmegen for their very good support.

Hamburg , in August 1996

Eckhard Bruns

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1. Introduction

Today the variety of TV-programs is growing nearly from day to day.

The software comes from several sources like the well known terrestrial broadcaster, cable systems, satellites, VCRs or security systems for example. But most the times only one TV-set with a large display is available at home.

So it's a clever solution to reduce the picture size of the interesting programs to 1/4 or 1/16 of the whole screen size and display it simultaneously with the main program.

For getting an overview of the actual running programs it is helpful to use the PiP concept as a program-search-tool. Together with the appropriate control-software its possible to divide the whole screen into 16 small pictures and fill each with a frozen picture of one of 16 several sources.

The device SAB9076/77 itself is able to handle two independent life pictures. Together with a fast switch it is possible to display two life pictures on a life background. The programs itself could be coded in different standards, PAL and NTSC for example. In fact a standard conversion is possible.
The device contains two independent acquisition channels incl. ADCs and data reduction and one display channel which contains the controlling of the external memory and the DACs.
The whole IC is controllable via IIC-bus.

The following application note first shows and explains several PiP-concepts in the 50Hz and 100Hz domain in part 2. Part 3 contains the roughly description of the PiP controller SAB9076/77 and how to control the device. Part 4 describes one of the possible applications. The chosen application is the stand-alone demoboard application. Part 5 gives some application hints for designing a PCB for the SAB9076/77.

2. Architectures of several PiP-applications

This chapter could give you an overview, what a wide range of possible applications for the PiPO-system exists. The following application proposals show the most interesting concepts, but the list must not be complete.

2.1 Two channel applications in 50Hz domain

The main blocks for a normal 50Hz video signal processing are the Tuner/IF, maybe an combfilter, a multistandard colour decoder (e.g. TDA 9141), some picture improvements, like PSI, CTI or Picture Booster and a video backend processor, like TDA 4780.

The easiest way to tune up this concept to a PiP-concept, is to build the system shown in Fig. 1 .

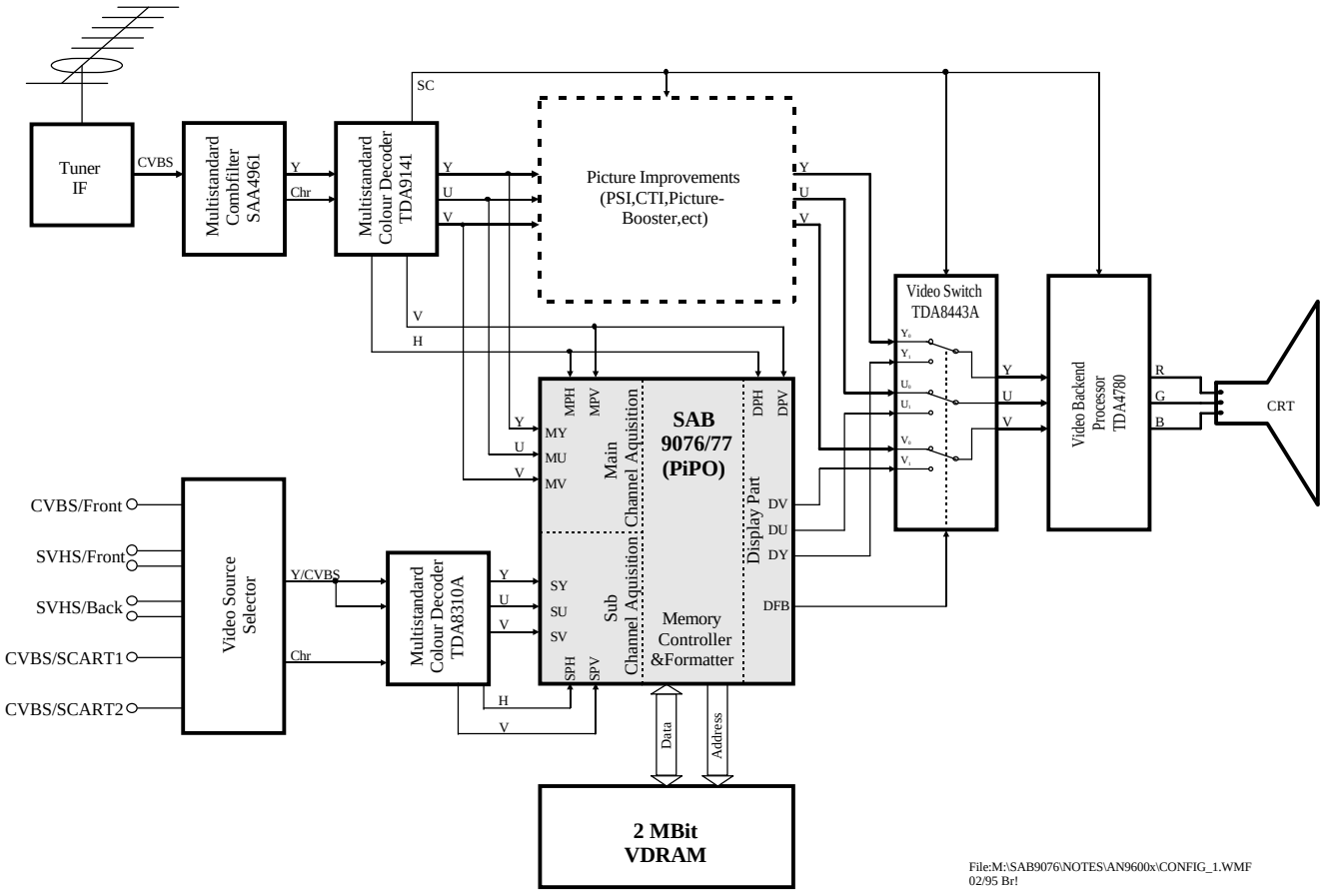

Fig.1 Two channel PiP-application in a 50Hz domain

The main signal path is marked as bold lines.

For switching between the main YUV-signals and the YUV-output signals from the PiP-system, a fast video switch has to be installed in the main signal path right before the video backend processor.
This fast switch is controlled by the DFB-signal provided by the PiP-Controller SAB 9076/77.

The main signal YUV_{main} is detached to provide the input signals for the main acquisition input of the PiP controller. The main acquisition part and the display control part of the PiP-controller are synchronized by the H- and V pulses of the colour decoder of the main signal path. This prevents the system for timing errors between the YUV_{main} signals and the YUV_{PiP} signals in front of the fast switch TDA 8443A.

The signal processing of the sub signal path contains a source selector and a multistandard decoder. The complexity of the video source selector depends on the amount of signals to be displayed in the PiP-windows. Fig. 1 shows a selection of several signals which are available in most of TV-sets nowadays.

1. CVBS/Front is the signal source provided by the Cinch plug at the front of most of the TV sets. It gives you the opportunity to display video signals from a camcorder in playback mode, an in-house video camera, an external video camera of an security system or from a game computer (e.g. Nintendo) in a PiP-window.
2. The signal inputs SVHS/Front and SVHS/Back gives you the opportunity to display video signals from SVHS camcorder or normal SVHS recorders in a PiP-window.
3. The CVBS/SCART inputs give you the opportunity to display the video signals of several sources, connected by a SCART cable to the TV set in a PiP-window, while the main program is still displayed on the screen. These sources could be:
   * VCR in playback or search mode, to position the tape, or to find a wanted scene or location on the tape.
   * SAT receiver, to observe the programs on other channels.
   * Pay-TV-decoder, to observe the programs in coded channels.

The output signals of the source selector could be normal CVBS-signals or Y/C signals from a SVHS-recorder for example.
The following multistandard colour decoder TDA 8310A is able to recognize and to handle both signal types automatically. The colour decoder for the sub channel delivers YUV signals with full luminance bandwidth for the sub acquisition input of the PiP controller and H- and V-pulses to synchronize the sub acquisition part of the PiP controller.

The PiP controller needs a 2MBit VDRAM (Video - DRAM) to store the data of the main- and sub pictures to be displayed in the PiP-windows. These VDRAM could be a TC528257J from Toshiba or a D482234 LE-70 from NEC. Both types are approved by Philips.

This concept offers you some features listed below:

1. The video sources of the sub channel can be displayed in a PiP-window.The PiP window can have three different sizes. The PiP window can be located everywhere on the screen. At the same time the main program is displayed on the whole screen in the background.
2. The video sources of the sub channel can be displayed in a PiP-window. At the same time the main program can be displayed in a second PiP window. The PiP windows can have three different sizes. The sizes are set for each window separately. Both PiP windows can be located everywhere on the screen and they may overlap each other. The background is filled with the main program.
3. The set shows the same features as 2), but the background is unique coloured.
4. The main program can be displayed via the PiP controller on the whole screen in life mode or frozen as a still picture.
5. The screen is splitted into two halfs, where one half displays the main program and the other half displays the sub program. Both pictures are horizontally reduced by factor two and have the fully vertical resolution. This mode is especially interesting for TV sets with 16:9 picture tube.

The list above describes only the normal modes. In manual mode there are much more features possible.

2.2 Three channel application in 50Hz domain

The concept describes under 2.1 operates with only one Tuner/IF section. If the sub channel should display a second broadcasted video signal, the tuner of a associated videorecorder has to be used for this feature. To be really independent from other units, a second tuner/IF section has to be implemented into the TV set. This is shown in the second concept approach in Fig. 2 .

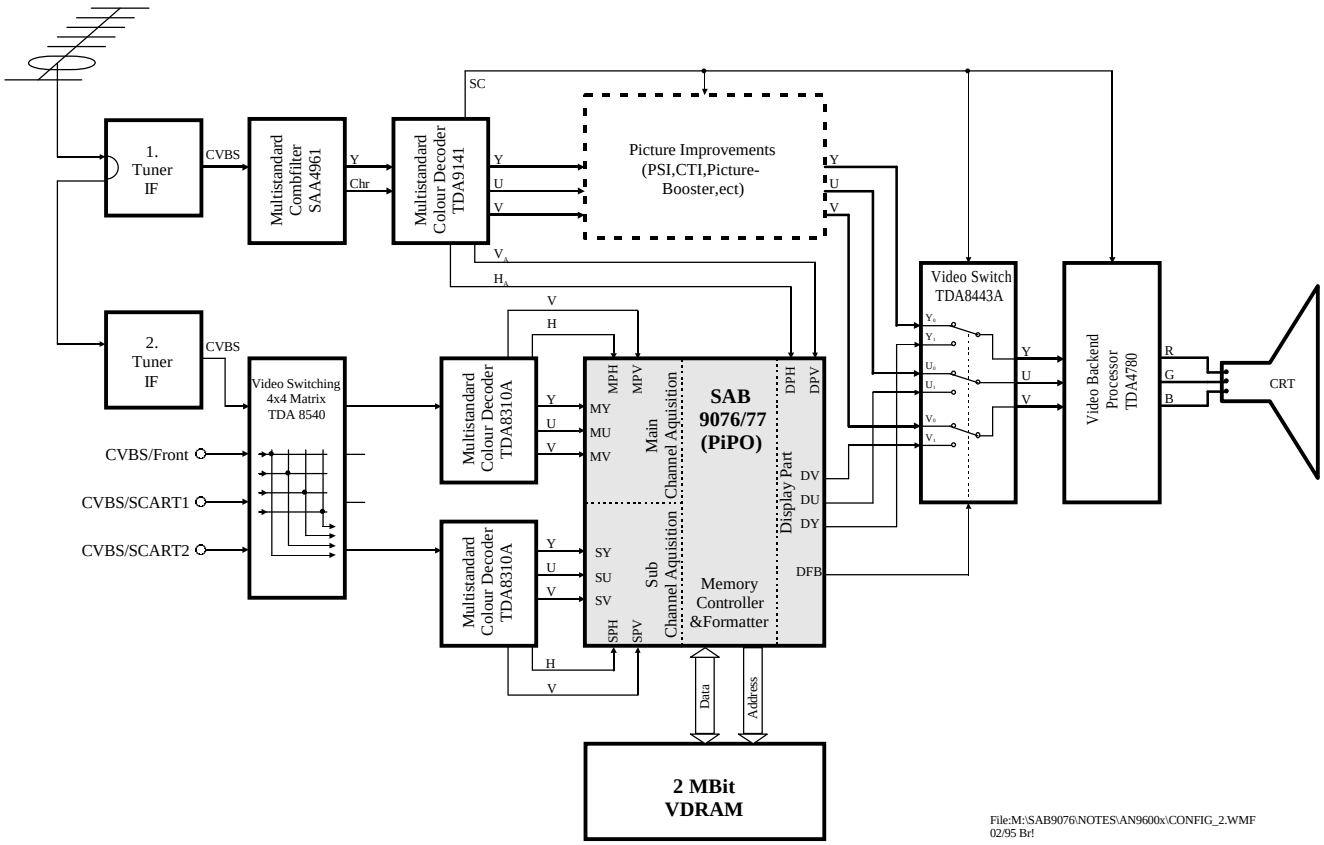

Fig.2 Three channel PiP-application in a 50Hz domain

The main signal path supports the main functions of the TV set like sound, pictures on the main screen and deflection, text and so on.

The second tuner gets the same RF input signal as the main tuner. The output of this “PiP-tuner” is a CVBS signal, which is fed into video switching matrix TDA 8540. The other inputs of the switching matrix could be supported from the front panel CVBS input or the SCART input of the back.

The next blocks in this PiP-signal processing chain are the multistandard colour decoders. The main acquisition part of the PiP controller has now its own colour decoder, which delivers the YUV signals and the H- and V-pulses for the main acquisition part.

The configuration of the colour decoder for the sub acquisition part, the PiP controller itself, the VDRAM and the fast switch before the video backend processor is exactly the same as described in chapter 2.1.

Due to the second tuner/IF section and the second colour decoder for the main PiP channel the whole PiP configuration is completely independent from the main signal path of the TV set. The only informations the PiP controller needs from the main signal channel of the TV set are the H- and V- pulses. These pulses have to be fed into

the display part of the PiP controller, to synchronize the display of the PiP windows and their contents with the deflection of the TV set.

This concept could be extended, if SVHS signal from the front and the back should be included in the PiP signal processing. The following Fig. 3 shows such an approach:

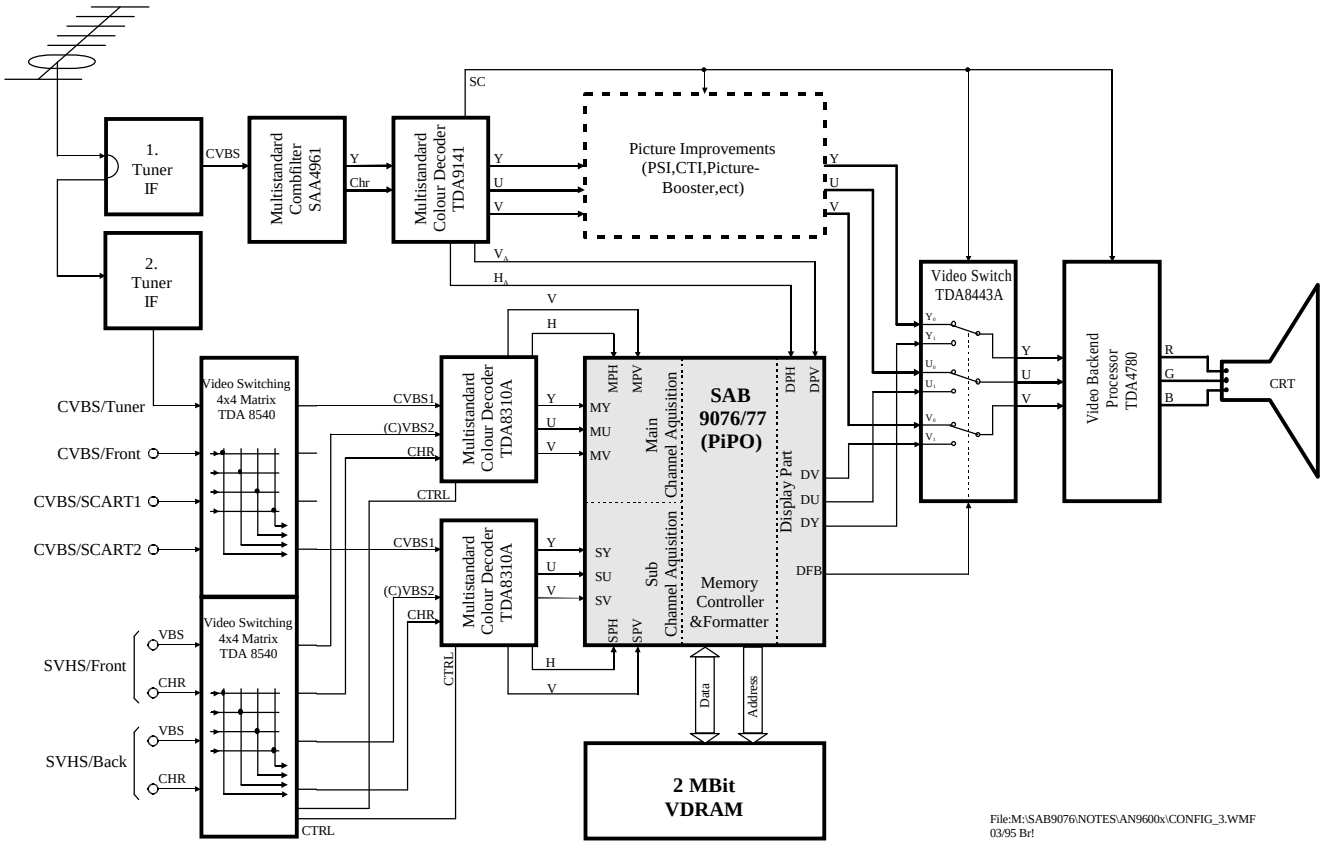

Fig.3 extended three channel PiP-application in a 50Hz domain

For applying the SVHS signals to the multistandard colour decoder, a second video switching matrix is located parallel to the first matrix TDA 8540. While the first matrix lead its output signals to the CVBS1 input of the colour decoders, the second matrix for SVHS signals feeds the CVBS2 and CHR inputs of the colour decoders. If the colour decoder TDA 8310A operates in automatic-mode, it could recognize whether there is a complete CVBS signal or a VBS signal on input CVBS2. If a VBS signal is detected, the internal filters will be switched into SVHS-mode and the device expects a chroma signal on the CHR input.

The selection between the CVBS inputs of the colour decoder is done via a DC-switching voltage, named CTRL in the Fig. 3 . The video switching matrix TDA 8540 provide control outputs which are programmable by IIC-bus.

So the complete selection (which SVHS signal to which colour decoder) and the mode control of the colour decoders (normal CVBS-mode or SVHS-mode) can be done via IIC-bus.

2.3 Applications for 100Hz - TV - concepts

The PiP signal processing can be implemented also in 100Hz TV concepts. Based on the former explained concepts, the PiP signal processing joins the main signal path before the 50/100Hz conversion.

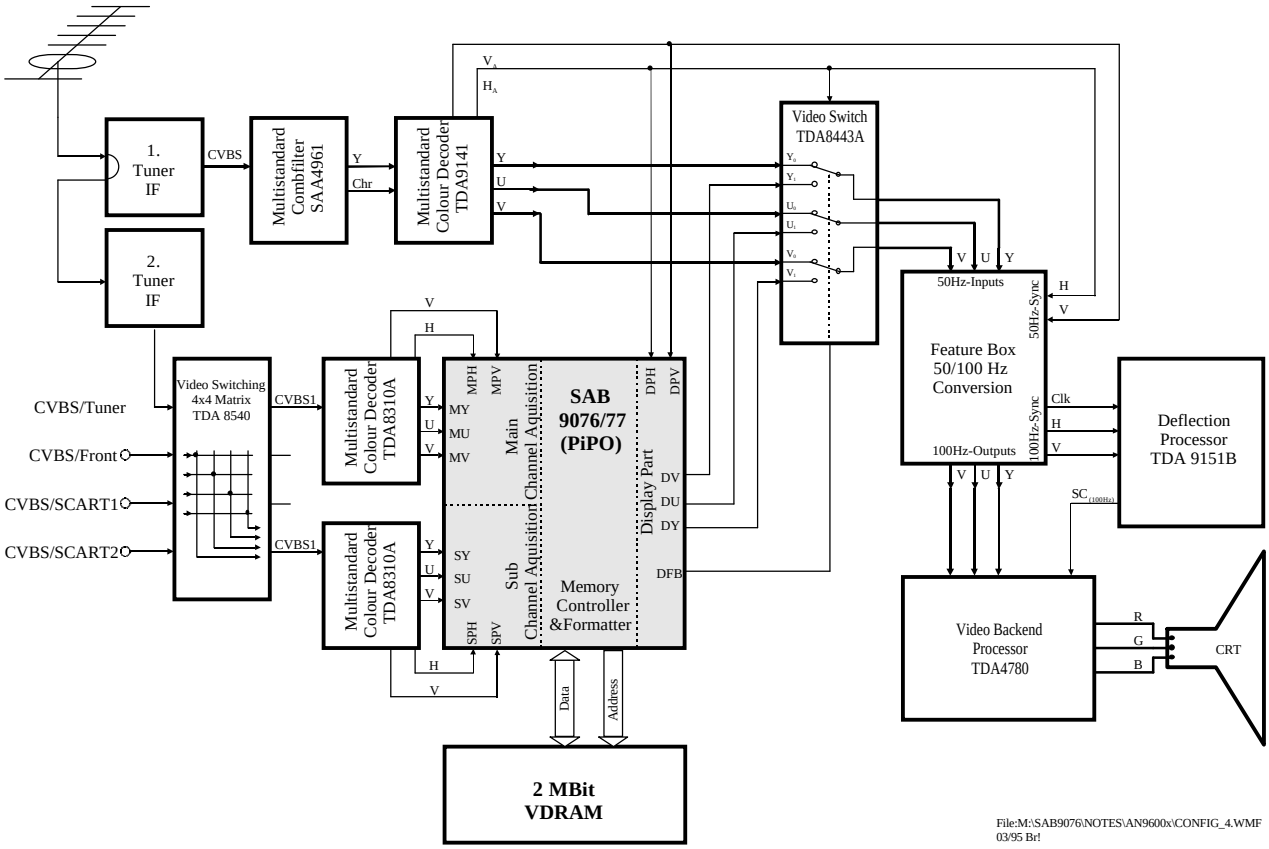

Fig.4 PiP signal processing in 100Hz TV concepts
Inserting the PiP signals on 50Hz domain

The PiP signal processing shown in Fig. 4 is still the same as explained in chapter 2.2 . The display part of the PiP controller is operating in the normal 50Hz domain. Therefore the synchronisation pulses DPH and DPV have to be provided by the main channel colour decoder TDA 9141. They are derived from HA and VA output signals of the TDA 9141.
The fast video signal switch TDA 8443A is positioned in front of the Feature Box for 50 -> 100Hz conversion. This IC is controlled by a DFB pulse with a frequency of 16 kHz (1*fH) .

The feature box needs the H- and V pulses of the main channel colour decoder for synchronisation on the 50Hz domain, too. It provides H- and V pulses and a linelocked clock on the 100Hz domain for devices, which are operating on the 100Hz domain, e.g. the deflection processor TDA 9151B. This device provides a 100Hz sandcastle pulse, to synchronize the video backend processor TDA 4780 in 100Hz mode.

The advantage of this concept is, that all the PiP pictures and their contents are normal video informations for the feature box. So the PiP pictures are included in the signal processing and interpolation of the 50/100Hz conversion. That means the PiP information will also displayed in the A,A*,B*,B mode as the video signal of the main signal path.
The disadvantage of this solution is that the PiP pictures can't be switched off, if the feature box is in freeze mode, because the PiP pictures are normal content of the incoming video signal.

2.4 Applications for VCR - concepts

The PiP signal processing concept can also be implemented into VCR concepts. For example, the customers wish to have an overview about the programs available via antenna/cable or satellite during the VCR is in play-back mode.
Due to modern integration technique, the video signal processing in video recorder has become more and more simple. So the complete signal processing can be done with a few ICs, which is shown in the upper part of the following Fig. 5 . The added blocks for the PiP signal processing are displayed in more details. It seems,that the expenditure for implementation the PiP concept is large, but that isn't true.

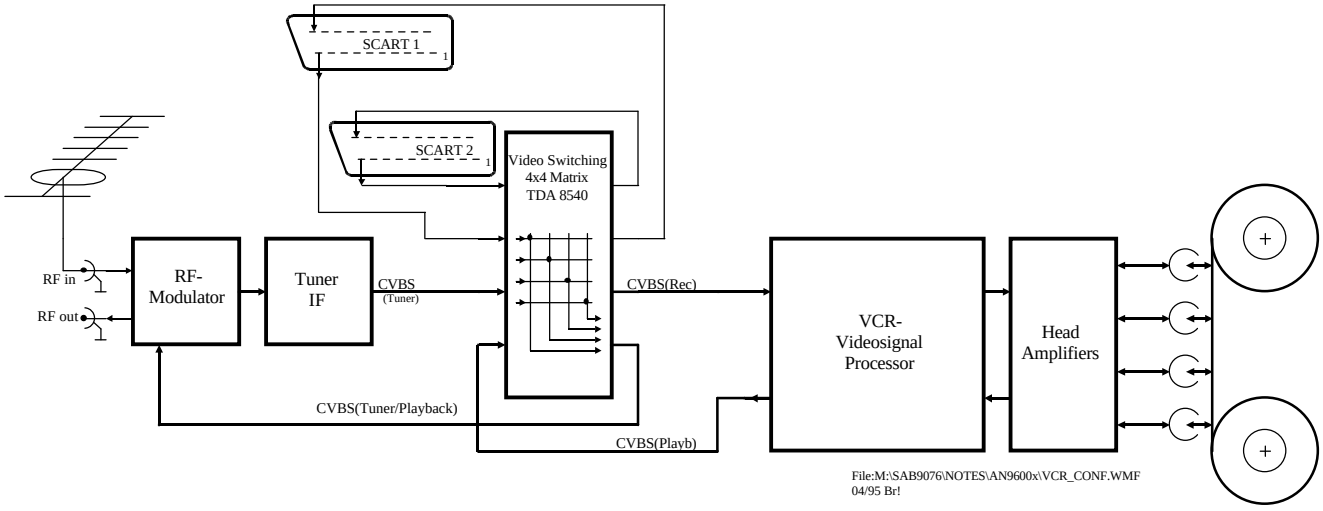

Fig.5 Video signal processing in VCR - concept

The normal signal path inside the VCR video signal processing is shown in bold lines.
The RF input signal is filtered inside the modulator and demodulated to a CVBS signal in the Tuner/IF section. Their output signal is fed into a 4X4 video switching matrix TDA 8540, to select the input signal for the VCR video signal processor. The other available input signals can be the CVBS signals of the SCART inputs coming from a satellite receiver or a pay-TV-decoder for example.
The selected signal [CVBS(Rec)] is processed by the VCR video signal processor and written via the head amplifiers to the tape.
In playback mode the information of the tape is read and processed back to a CVBS signal [see Fig. 5 CVBS(Playb)] by the VCR video signal processor. This signal is lead to the switching matrix again to distribute it to the SCART connectors and the modulator. The modulator converts the CVBS signal back to a RF signal to supply TV sets, which have no SCART inputs.

The implementation of the PiP signal processing has to fulfil two major requirements:

1. The main video signal processing path should be touched as less as possible.
2. The implemented PiP signal processing should be as flexible as possible.

The result is shown in Fig. 6 .

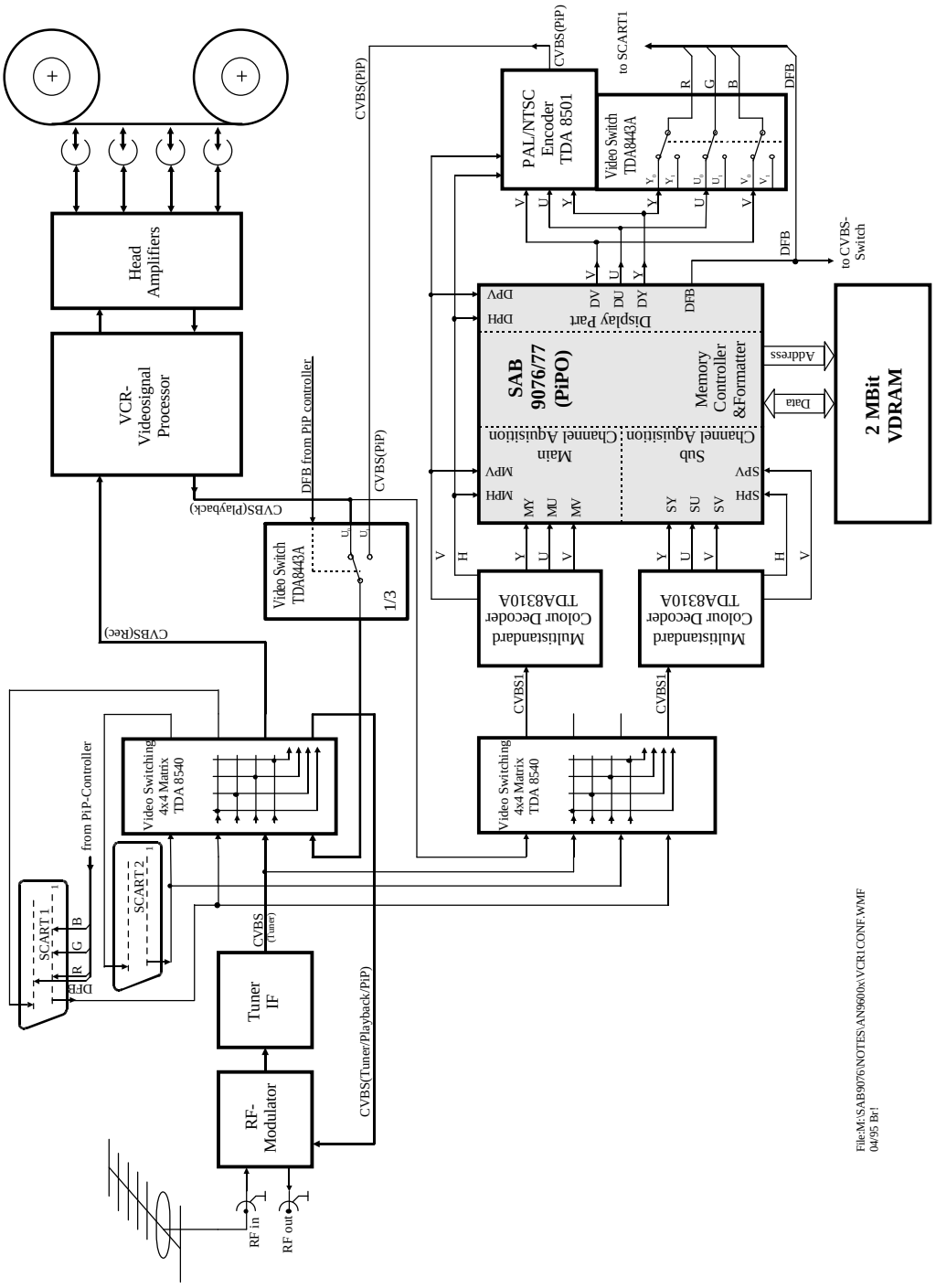

Fig.6 First implementation of PiP signal processing into a VCR - concept

The first requirement is fulfilled with insertion of only one fast switch TDA 8443A into main signal path. This fast switch selects between the output video signals of the VCR video signal processor and the PiP signal processing. In fact the PiP CVBS signal is inserted into the CVBS(Playback) signal. The completed signal is fed into the video matrix of the VCR main path, to distribute it to the modulator **and** to the SCART connectors.

The second requirement is fulfilled by the completely parallel signal processing of the PiP path.The kernel of the PiP signal processing is the well known configuration of the two multistandard colour decoder, the PiP controller and the VDRAM.

To insure the independence of the PiP signal processing from the VCR main signal path, the input signals for the colour decoders are selected by an extra video switching matrix. The input signals for this matrix are delivered from the Tuner/IF section, the SCART sockets and the VCR video signal processor.

The selected CVBS signals are lead to the colour decoders and converted into YUV signals. The YUV signals of the main and sub channel will be processed inside the PiP controller.
The main acquisition part is synchronized by the main colour decoder and the sub acquisition part is synchronized by the sub colour decoder. The display part is locked to the main acquisition part in this configuration, but other solutions are possible, too. It always has be ensured, that the display part of the PiP controller is synchronized to that video signal which is actual carried out as the VCR main signal.

The output signals of the PiP controller have to be converted to a CVBS signal first, before they can be inserted into the CVBS(Playback) signal of the VCR video signal processor. This is done by the PAL/NTSC Encoder TDA8501 for example. This device has to be locked to the same H - and V synchronisation pulses as the display part of the PiP controller.The completed CVBS(PiP) signal is connected to the second input of the fast CVBS switch. This switch is controlled by the DFB pulse coming from the PiP controller.

If the PiP controller is switched into OFF state, the DFB pulse has a constant state and the output signal of the VCR video signal processor is connected continuously to the output of this fast switch. In the case of displaying a coloured background together with the PiP pictures, the DFB pulse has the constant opposite state. So the output signal of the VCR video signal processor is blanked.

In normal operation mode the fast switch is toggling between the two input signals. In playback mode the PiP signal CVBS(PiP) is inserted into the video signal coming from tape. If the VCR operates in stop - or tuner mode, the VCR video signal processor must have an EE-mode [CVBS(Rec)=CVBS(Playback)] to ensure the connection of the selected input signal to the first input of the fast switch.
This configuration allows, for example, to display the video signal of the SCART2 connector as the main signal and the tuner-CVBS signal as PiP signal. Both together could be lead to the SCART1 connector as output signal.

As an option Fig. 6 shows the RGB configuration. The output signals of the PiP controller are connected to a second fast switch IC TDA 8443A. This IC operates as an YUV -> RGB matrix only. Its output signals together with the DFB pulse are connected to the RGB and BLANK pins of the SCART1 connector.
This configuration allows the inserting of the PiP signals into a synchronized CVBS signal inside a monitor, which is connected to the SCART1 socket.

For the case, that the VCR video signal processor couldn’t operate in an EE-mode, the location of the CVBS fast switch has to be changed. The varied configuration is shown in Fig. 7 .

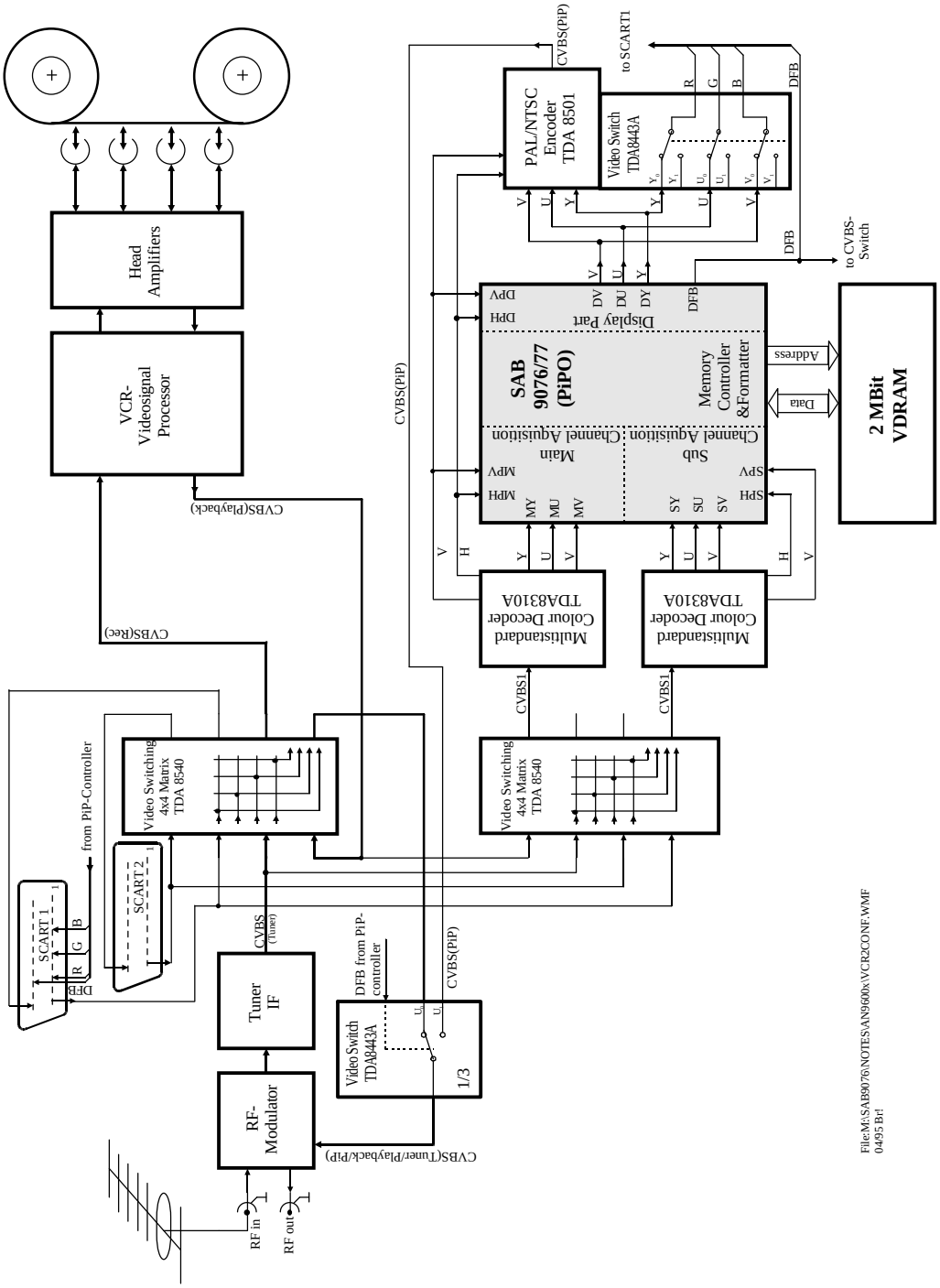

Fig.7 Second implementation of PiP signal processing into a VCR - concept

This configuration allows to insert the PiP CVBS signal into a selected incoming CVBS signal from the tuner, SCART1 connector, SCART2 connector or into the CVBS(Playback) signal from the VCR video signal processor. The disadvantage of this concept is, that the combined signal is fed only to the modulator and not to the SCART connectors. This effect could be avoided by adding a third video switching matrix.

2.5 Applications for SAT - Receivers

Modern satellite receivers, especially twin-receivers offer the opportunity to receive two independent satellite signals and distribute them to several devices like TV sets, descrambling (Pay-TV) decoders or VCRs.
So these receivers are interesting for the implementation of a PiP signal processing.

The basic concept of a Twin-Satellite receiver is shown in Fig. 8 .

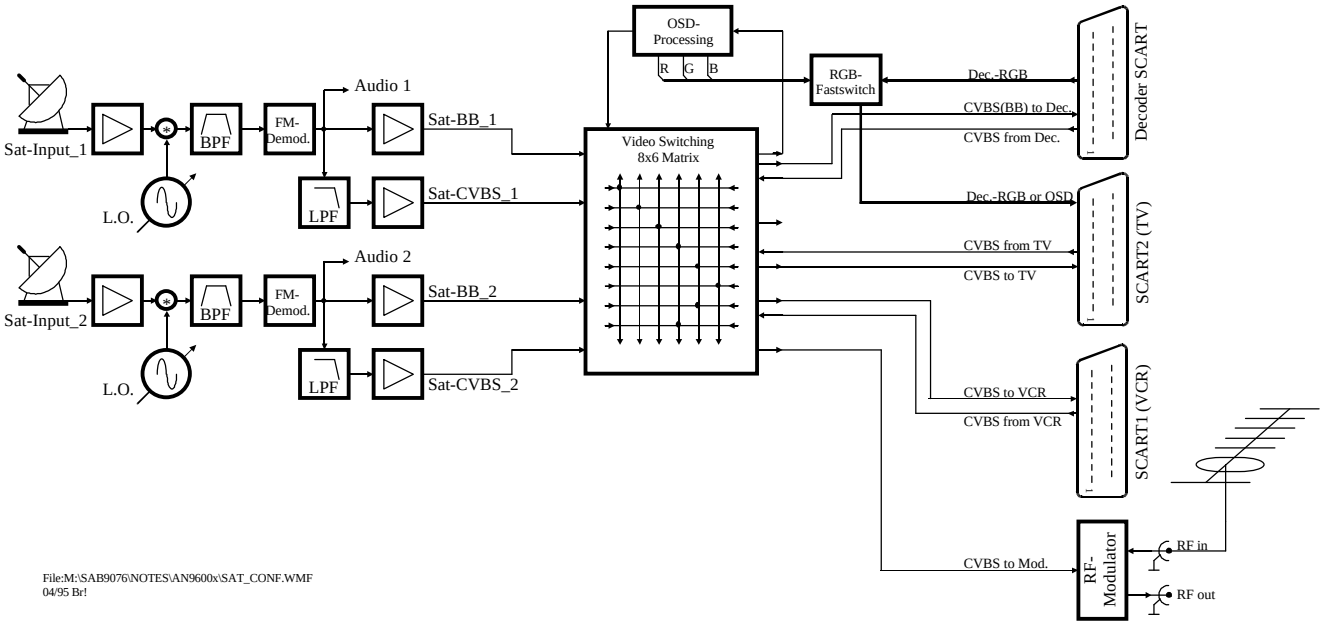

Fig.8 Blockdiagram of Twin-Satellite receiver

A Twin-Satellite receiver has two similar frontends. They convert and demodulate the incoming satellite signals to a normal CVBS signal (Sat-CVBS_1,2). The second outputs of these frontends are the baseband outputs Sat-BB_1,2. The baseband signals are not bandwidth limited and contain informations, which are necessary for the descrambling decoders.
All four signals are fed into a video switching matrix.

The video switching matrix delivers the selected baseband signal (Sat-BB_1,2) to the SCART connector, where the descrambling decoder is connected to. Most of the descrambling decoders give back the decoded TV signal as a normal CVBS signal and as RGB signals. The CVBS signal from the decoder is fed into the matrix to be distributed to the TV-SCART, the VCR-SCART or to the RF-modulator.
The RGB output signals of the decoder are mixed with the RGB signals from the OSD-block and lead to the TV-SCART connector.

The matrix serves also the TV-SCART connector and the VCR-SCART connector with incoming and outgoing CVBS signals.

One of the CVBS signals (Sat-CVBS_1,2 or CVBS from decoder or CVBS from TV or CVBS from VCR) can be selected for the RF-modulator.

The implementation of the PiP signal processing has to fulfil again the two major conditions:

1. The existing concept of the SAT-receiver should be touched as less as possible.
2. The expenditure of the additional circuitry for the PiP signal processing should be small.

These conditions are fulfilled with the concept shown in Fig. 9 .

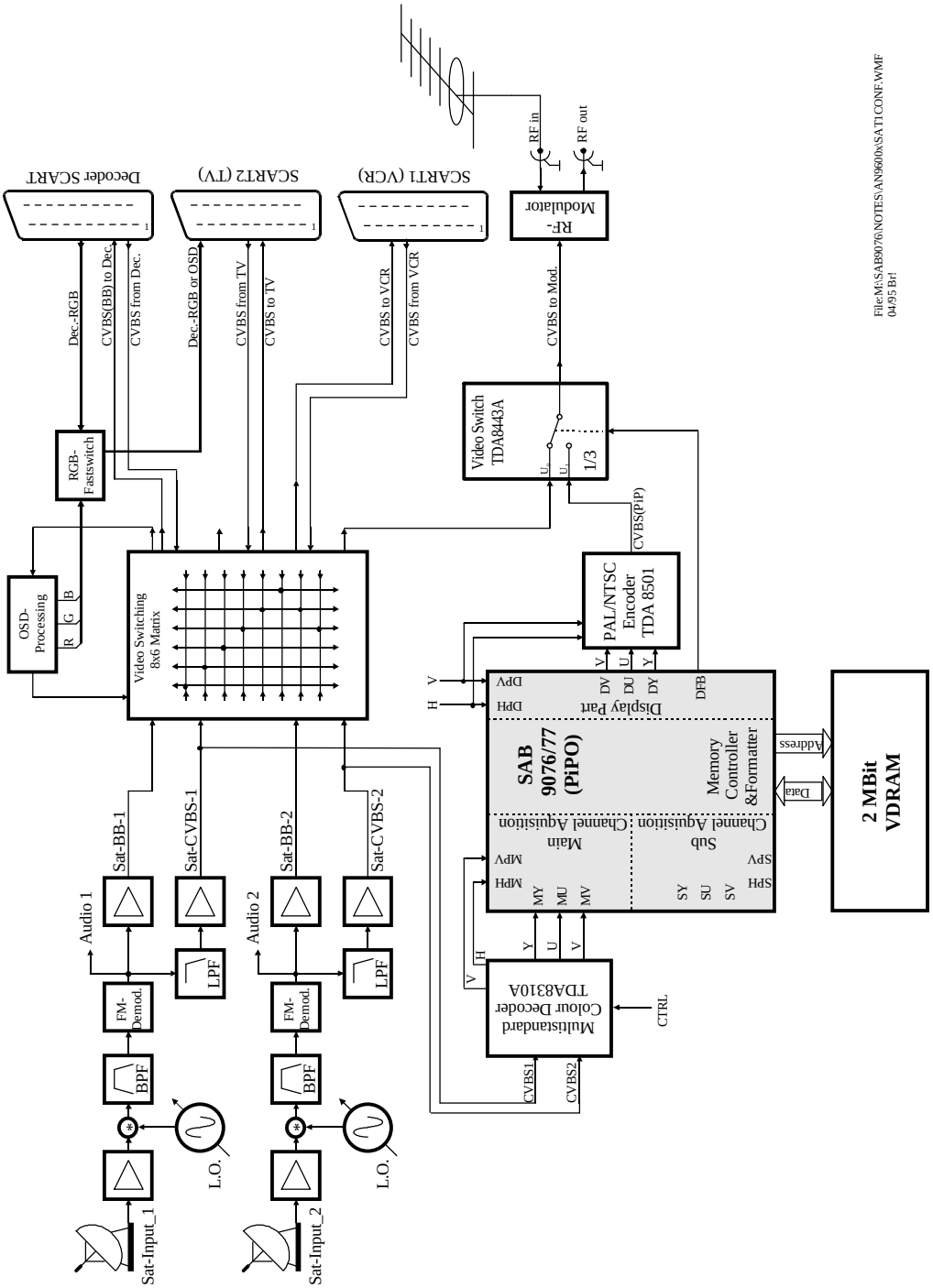

Fig.9 Simple implementation of PiP signal processing in an SAT-receiver concept

In this simple application the demodulated satellite input signals (Sat-CVBS-1,2) are connected to the two inputs of one multistandard decoder TDA 8310A of the PiP kernel. This application only uses the main acquisition channel of the PiP controller to display the actual SAT program of either input 1 or input 2. The selection between the inputs of the multistandard decoder (CVBS1 <-> CVBS2) has to be done by a control voltage, issued from a IIC bus device.
The selected input CVBS signal is converted into YUV-signals and the synchronization pulses are generated, too.The YUV signals are processed by the PiP controller and the H- and V-pulses synchronize the main acquisition part. The display part of the PiP controller as well as the PAL/NTSC encoder TDA 8501 will be synchronized by H- and V-pulses derived from the CVBS signal where the CVBS(PiP) signal should be inserted into.

The encoder is necessary to convert the processed YUV signals back to the CVBS domain.

The complete output signal of the PiP kernel [CVBS(PiP)] is lead to a fast CVBS switch TDA 8443A which inserts the CVBS(PiP) signal into a selected CVBS signal, intended to be modulated by the RF-modulator. The fast CVBS switch is controlled by the DFB signal coming from the PiP controller. Every time this signal is active, the switch leads the CVBS(PiP) signal to the RF-modulator.

With this configuration the user can observe the sat-inputs while he's watching a video film of a VCR for example. The monitor he's watching, has to be switched into RF-mode and to the channel, the SAT receiver is transmitting on.

The concept was kept intentionally simple to keep the expenditure as low as possible. The price for the simplicity is less flexibility. To get more flexibility, the system can be extended as shown in Fig. 10 .

The extended application has an additional multistandard colour decoder TDA 8310A for the sub acquisition channel and the fast CVBS switch is performed as a double switch. The second colour decoder gives the opportunity to display the two independent satellite input signals at the same time together with a third CVBS signal as background.
In this application the connections between Sat-CVBS1,2 and the inputs of the main/sub colour decoders are fixed. So the input switch control of the main colour decoder is obsolete.

The processed PiP output signals are converted to the CVBS domain by a PAL/NTSC encoder TDA 8501 like in the concept before. The completed signal [CVBS(PiP)] is lead now to two switches which insert the CVBS(PiP) signal into the selected CVBS signal for the RF-modulator and in parallel into the selected CVBS signal for the TV set, connected to the SAT receiver via the SCART2(TV) connector.

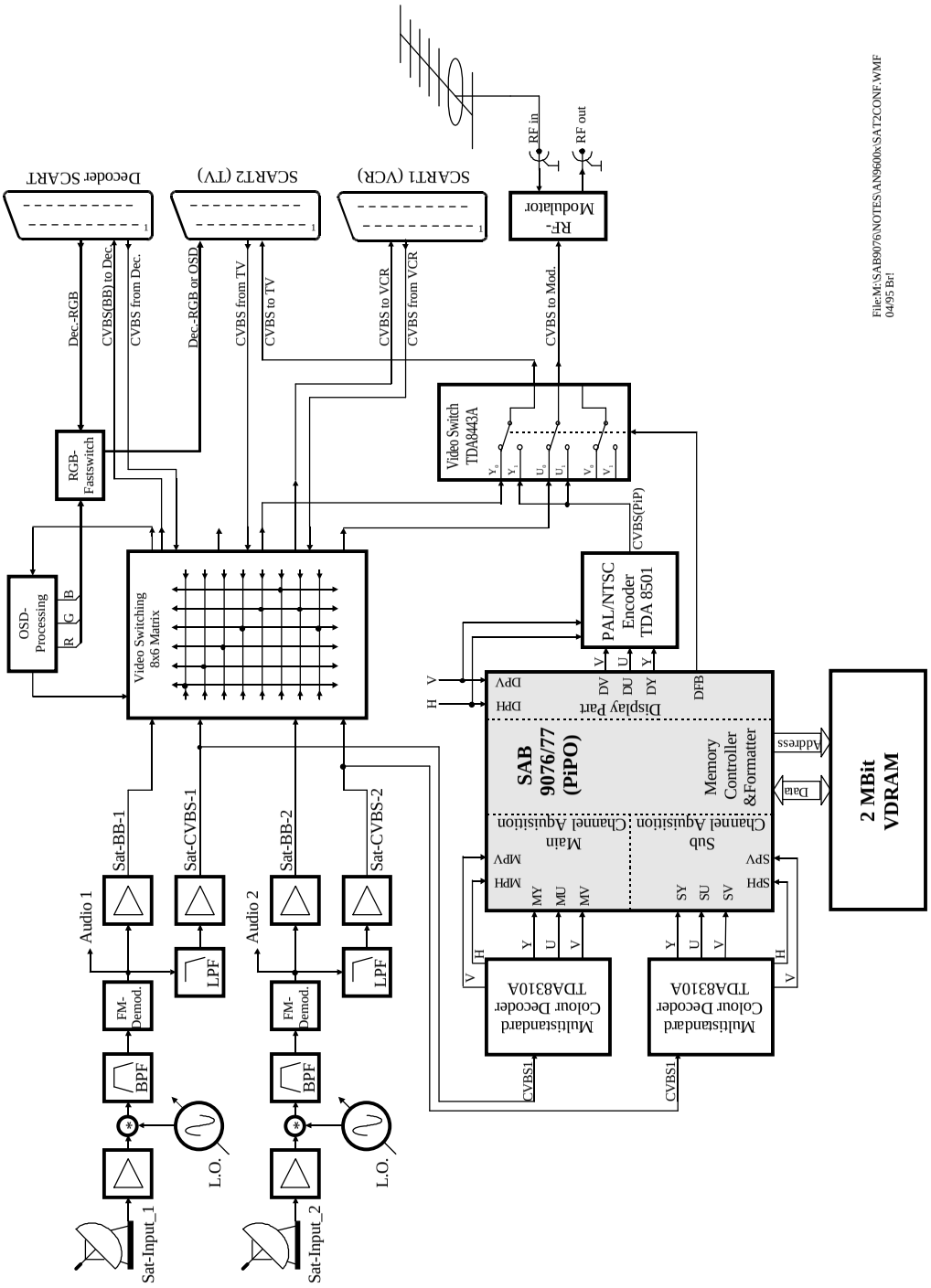

Fig.10 Extended application of PiP signal processing in an SAT-receiver concept

The both concepts described before are able to display only the SAT input signals as PiP pictures in their PiP windows. If more program sources should be available for the PiP processing, the flexibility has to be extended again. This is shown in Fig. 11 .

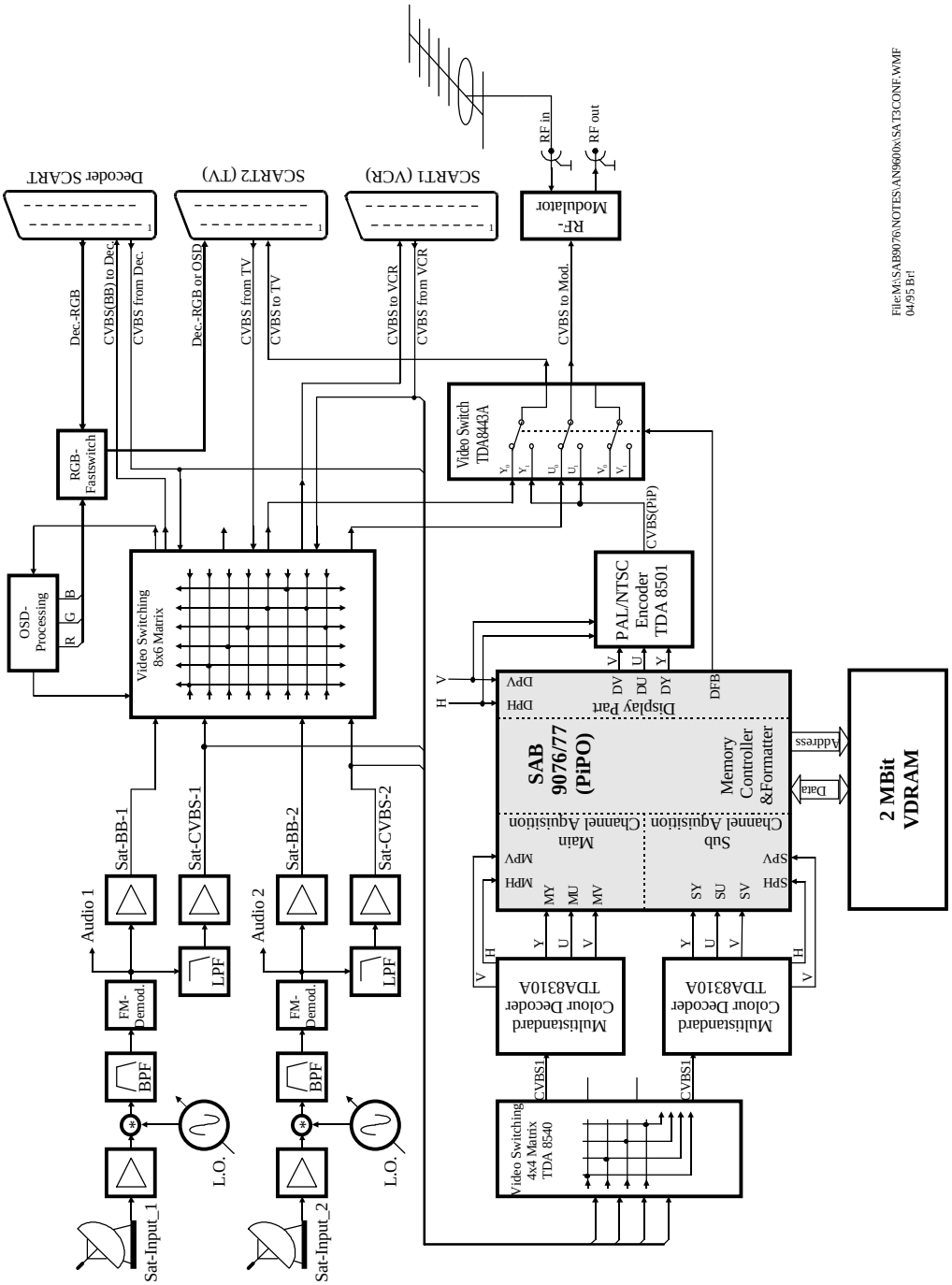

Fig.11 High end application of PiP signal processing in a SAT-receiver concept

The PiP signal processing is now extended by an additional video switching matrix to select the input CVBS signals for the multistandard decoders of the PiP kernel. With this configuration the two SAT input signals (Sat-CVBS1,2) and the output signals of the descrambling decoder (CVBS from Decoder) and the VCR (CVBS from VCR) can be selected as input signals for the PiP processing.
The backend of the PiP signal processing is still the same as described before.

3. Short Description of the PiP-Controller SAB 9076/77

In this report only a short description of the PiP controller SAB 9076/77 and it's features are given. A more detailed description is given in the application note AN96041 "Picture-in-Picture Controller SAB 9076".

3.1 Blockdiagram

The PiP controller consists of three independent major parts:

1. Sub channel acquisition part for sampling and filtering the sub channel video signals.
2. Main channel acquisition part for sampling and filtering the main channel video signals.
3. Display part for providing the processed video data with the correct timing in respect to the display H- and V pulses. The blocks for formatting and reformatting the video data as well as the complete memory controller and the A/D conversion are included in this part, too.

Fig. 12 shows the top shell block diagram of the PiP controller SAB 9076/77.

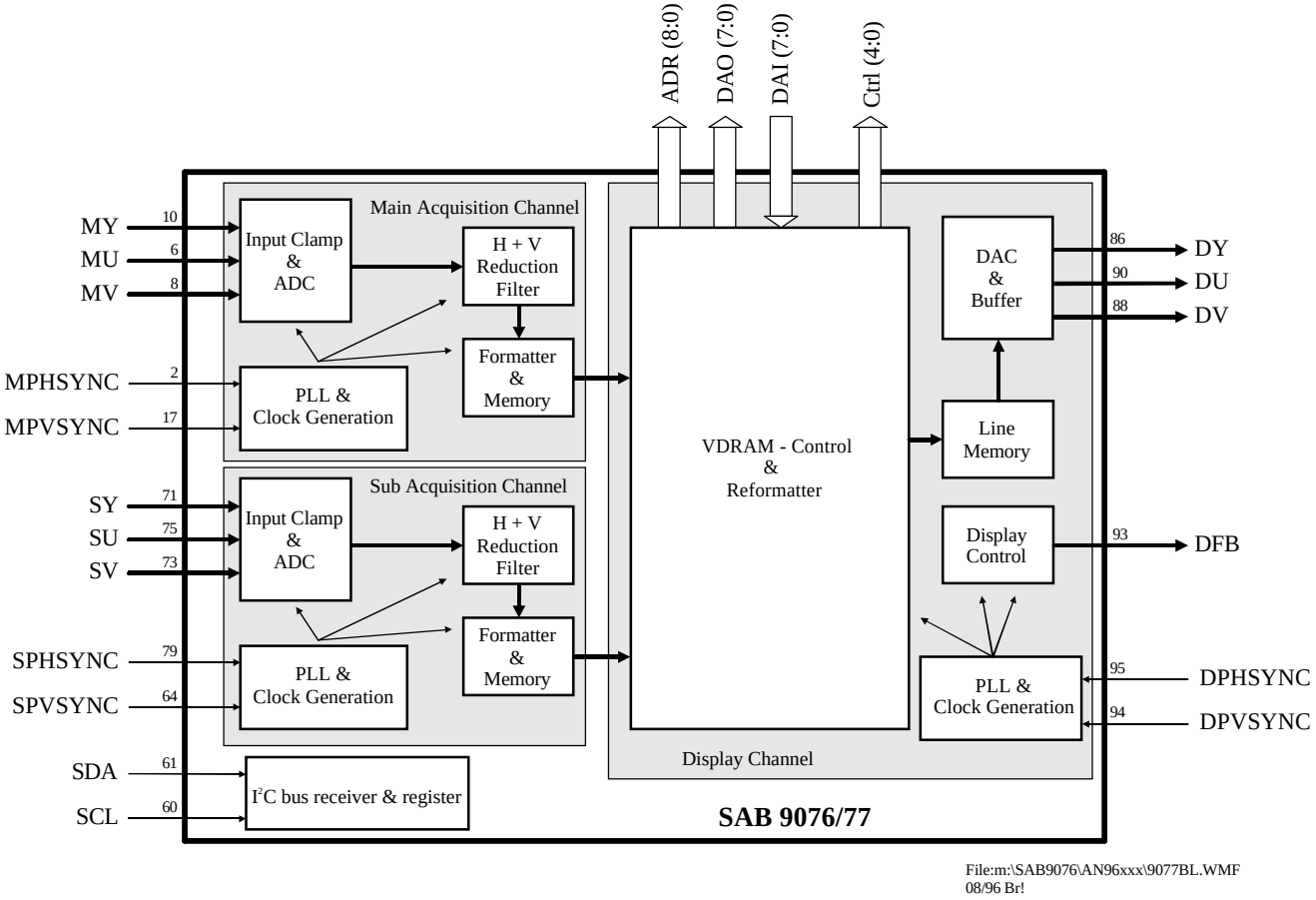

Fig.12 Top shell block diagram of the PiP controller SAB 9076/77

3.2 Description of Blocks

The main - and the sub channel acquisition part are identical.
The incoming YUV signals are sampled into the 4:1:1 data format. The bandwidth of the input signals is expected to be limited to 4.5 MHz for the luminance and 1.125 MHz for the chroma difference signals.
The Y input signal is clamped and sampled with a 1728 • f_H clock (~ 27 MHz). The data stream is then filtered and down sampled to the internal data rate of 864 • f_H (~13.5 MHz).
The U- and V input are first multiplexed and then sampled with a 432 • f_H clock (~ 6.75 MHz). Same as the luminance data, they are down sampled to the half pixel rate of 216 • fH (~ 3.375 MHz).
Behind the down sampling the data reduction filters are attached. They reduce the data in horizontal and vertical direction in respect to the desired PiP size. The remaining pixels/line and lines/PiP depend on the selected PiP-size and are listed below in Table 1 .

TABLE 1 Pixels and Lines of PiP in respect to desired reduction

Condition	Reduction - Factor			
Horizontal reduction	1	½	1/3	¼
Pixel per Line	672	336	224	168
Vertical reduction	1	½	1/3	¼
Lines per PiP in NTSC	228	114	76	57
Lines per PiP in PAL	276	138	92	69

The reduced data stream in the 4:1:1 format has to be formatted to meet the data format of the external memory. The complete processed data are stored in an internal line memory and provided to the VDRAM controller.

The complete timing (clock generation, sampling, filtering etc.) is synchronized in horizontal and vertical direction by the applied H- and V pulses [M(S)PHSYNC and M(S)PVSYNC]. M stands for “main channel” and S stands for “sub channel”.
With the acquisition fine positioning (I^2C bus register value) added to a fixed system constant, the start of the acquisition can be controlled in horizontal and vertical direction, independent for each acquisition channel.

The VDRAM controller is responsible for the complete data handling to and from the external memory. This block is a part of the IC’s display channel and it’s timing is determined by the display control block. The data transmissions between the acquisition parts and the external memory has a different priority than the data transmission from the external memory to the display part of the IC.
Providing correct data to display part has always the highest priority. The necessary processing time of the remaining blocks of the display part like reformatter, upsampling or D to A conversion has to be taken into account. In the time slots, where no data have to be fetched from the external memory, the provided data from the acquisition part can be written to the external memory. Due clever data handling a synchronization between non synchron video sources of the main- and the sub acquisition channels and the timing of the environment, the PiP application is implemented in, is obtained.
The data read back from the memory have to be reformatted to the 4:1:1 format. The data stream has a pixel rate of 864 • $f_{H(Display)}$ (~ 13.5 MHz). This data stream is fed to the line memory.
The VDRAM controller gets it’s start- and control signals from the display PLL and the display controller. These blocks are locked to the timing raster of the environment, the PiP application is implemented in.The synchronization is obtained by the attached H- and V pulses DPHSYNC and DPVSYNC.
The complete address generation for both, writing the processed data to the memory and reading back data for the display part as well as control signal generation for the external memory are included in the VDRAM controller.

The reformatted data stream is intermediate stored in the line memory of the display part to provide the data for

the upsampling stage. The upsampling stage generates a pixel rate of 1728 • $f_{H(Display)}$ (~ 27MHz) by interpolation.
This data stream is converted back to the analog domain and buffered by three output buffer stages. The display controller generates the output signal DFB, which indicates when the output signals DY, DU and DV have valid video signals. Borders of PiP pictures are valid video signals, too.

3.3 PiP modes

The architecture of the PiP controller allows a very flexible controlling of the two acquisition- and the display channel, independent of each other. So a lot of several modes are possible, but a subset of seven modes is fixed and can easily be set by I^2C bus. The standard PiP modes with their associated presettings are listed below in Table 2 .

TABLE 2 PIP Modes and presettings

PIP Modes			Reduction Factors				PiP positioning			
			Sub Channel		Main Channel		Sub Channel		Main Channel	
Name	Figure	Mode	Hred	Vred	Hred	Vred	SDhfp	SDvfp	MDhfp	MDvfp
SP	SP Small	0000	1/4	1/4	-	-	-	-	-	-
SP	SP Medium	0000	1/3	1/3	-	-	-	-	-	-
SP	SP Large	0000	1/2	1/2	-	-	-	-	-	-
SP	SP Small	0000	-	-	1/4	1/4	-	-	-	-
SP	SP Medium	0000	-	-	1/3	1/3	-	-	-	-
SP	SP Large	0000	-	-	1/2	1/2	-	-	-	-
DP	DP	0000	1/2	1/2	1/2	1/2	03h	46h	57h	46h
DP	Twin PIP	1001	1/2	1/1	1/2	1/1	03h	05h	57h	05h
MP3L	POP-Left	0010	1/4	1/4	-	-	08h	10h	-	-
MP3R	POP-Right	0010	-	-	1/4	1/4	-	-	72h	10h
MP3D	POP-Double	0010	1/4	1/4	1/4	1/4	08h	10h	72h	10h
MP7	POP-Double	0011	1/4	1/4	-	-	03h	05h	-	-
MP8	MP7	0011	1/4	1/4	1/2	1/2	03h	05h	44h	20h
MP4	Quatro	0001	1/2	1/2	1/2	1/2	03h	05h	03h	77h
MP9	MP9	0100	1/3	1/3	1/3	1/3	03h	05h	51h	3Bh
MP16	MP16	0101	1/4	1/4	1/4	1/4	03h	05h	03h	05h
MP16	MP16 Mix	0110	1/4	1/4	1/4	1/4	03h	05h	03h	77h
FFS	Full Field Still	0000	1/1	1/1	-	-	03h	05h	-	-
FFS	Full Field Still	1000	-	-	1/1	1/1	-	-	03h	05h
MAN	Manual	X111	x	x	x	x	x	x	x	x

The abbreviations are:

TABLE 3 Abbreviation of standard PiP modes

Abbreviation	Meaning	Remark
SP(S/M/L)	Single PiP	S = small (1/4); M = medium (1/3); L = large (1/2)
DP	Double PiP	two large PiP's on coloured background
POP	Picture on Picture	
MP(n)	Multi - PiP	(n) = number of PiPs (3,4,7,8,9 or 16)

The layouts of the several PiP modes are shown in the following Fig. 13 and Fig. 14 .

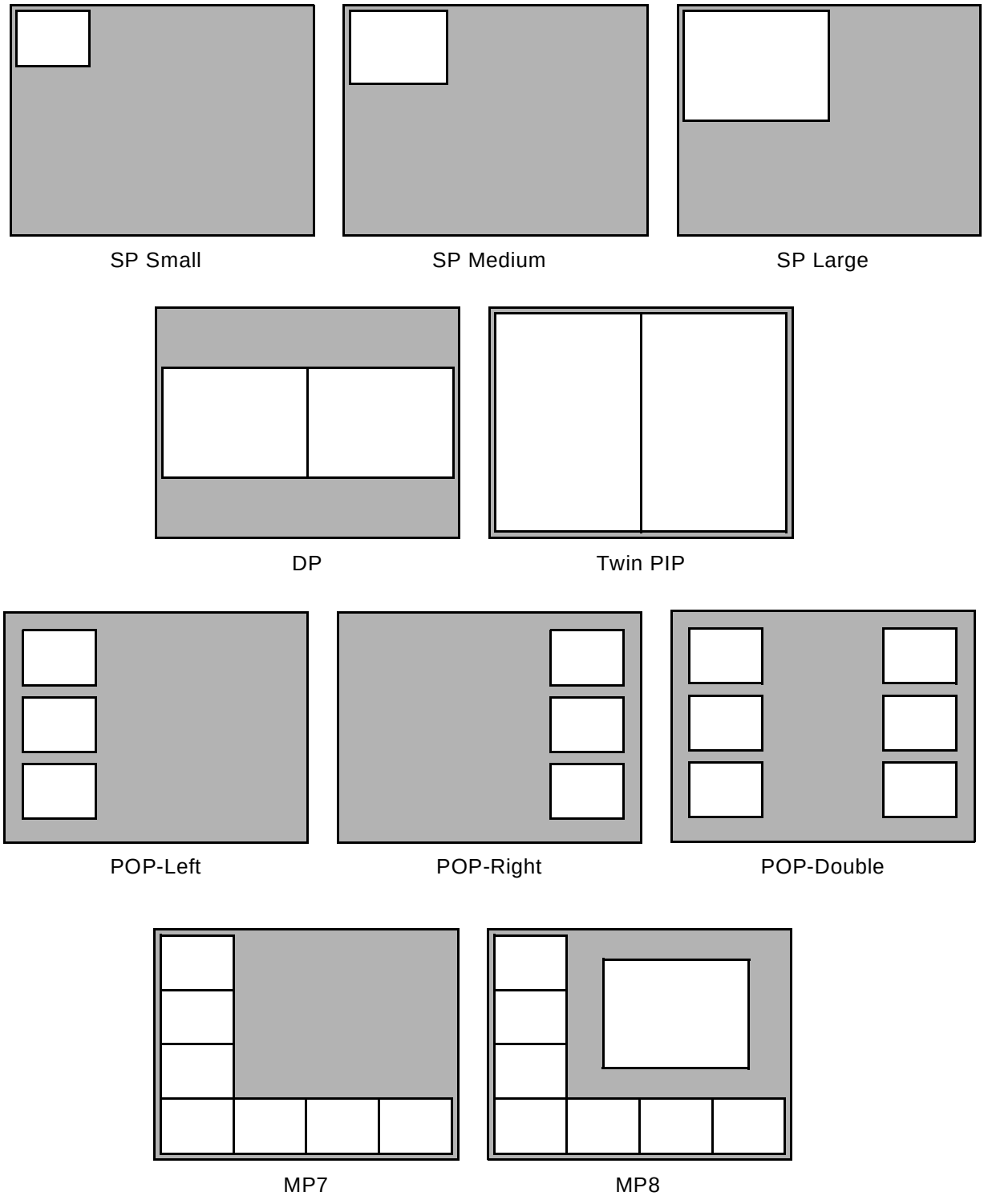

Fig.13 Pip modes 1

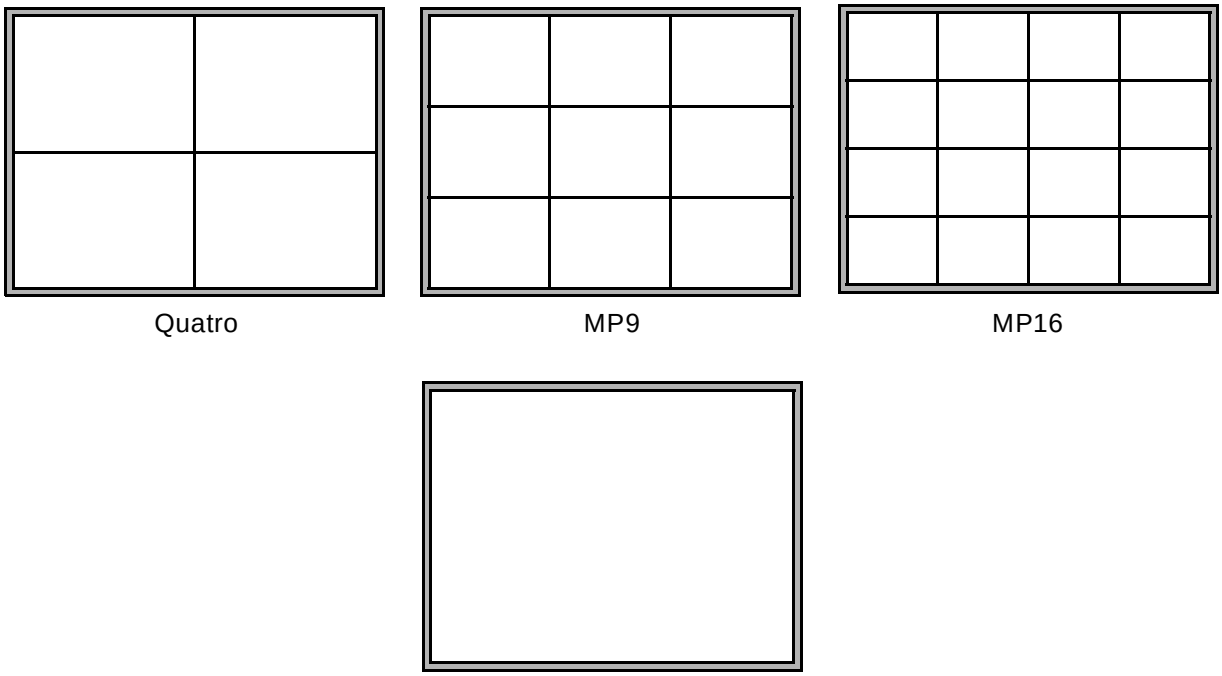

Fig.14 Pip modes 2

The standard PiP modes are selected by the corresponding mode bits of the I2C bus register. To display the PiP pictures in the arrangement shown above, the correct setting of the main/sub display positioning bits is necessary. The required values are listed in Table 2 in the right four columns. The basics of PiP picture positioning is explained in the chapter below.

3.4 Background- and PiP positioning

The PiP background is an area of 696 pixel for both PAL and NTSC and 238 lines for NTSC or 286 lines for PAL. The environment, the PiP application is implemented in has a display area which is determined by it's H- and V pulses. These synchronization pulses (DPHSYNC & DPVSYNC) are fed to the display part of the PiP controller, too and determine the basic display area of the PiP controller. This is shown in Fig. 15 .
The PiP background area is locked to the display area and can be shifted in horizontal and vertical direction. The shift is determined by the values in the corresponding I^2C bus registers BGhfp and BGvfp. The maximum shifting range is 64 pixel in horizontal and 36 lines in vertical direction.
Inside the background area the PiP pictures are defined. Their starting points (upper left corner) are defined by the values in the I^2C registers MDhfp and MDvfp for the main channel and SDhfp and SDvfp for the sub channel. The PiP pictures may overlap, but they can't leave the background area.
Normally the background is transparent, so the life picture of the TV set is visible. Then the PiP pictures lay over the TV-set's life picture.
The background also can be coloured with several colours. In this case the TV-set's life picture is blanked and the PiP pictures occur on an unique background.

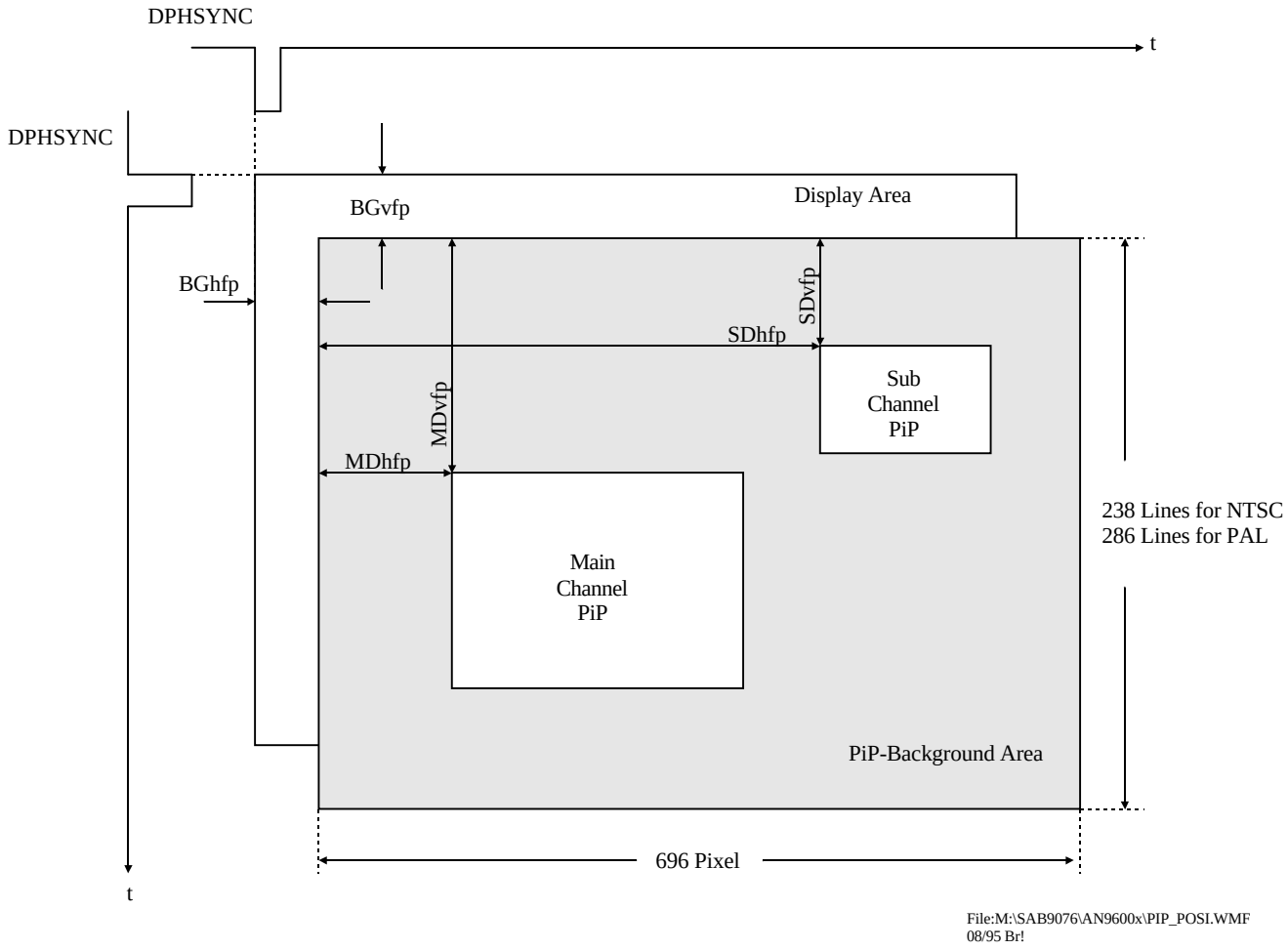

Fig.15 Background and PiP positioning

3.5 I²C-Registers

The PiP device SAB 9076/77is fully controllable by I²C bus. The device address can be selected between $2C_{HEX}$ and $2E_{HEX}$ by hardware configuration. For default the I"C bus address is $2C_{HEX}$. The evaluation- and control software is written for the I2C bus address $2C_{HEX}$, too. In the evaluation- and control software the address is fixed and can't be changed.
In normal operation mode the subadresses 00_{HEX} to 18_{HEX} are valid. If the manual mode is selected, the subaddresses 20_{HEX} to 32_{HEX} become accessible.
The PiP controller contains a I²C bus receiver and can't send any information back to the I²C bus master. The data transmission has to be made accordingly to the standard I²C bus protocol.

An overview of the I2C bus registers and their content is given in Table 4 .

TABLE 4 Overview of I^2C bus registers for normal operation modes

Sub Address	Data Bytes							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00H	MPIPON	SPIPON	MFreeze	SFreeze	MCopy	$PiPMode_{(2:0)}$		
01H	-	-	M1FLD	S1FLD	NiPCoff	DNonInt	MNonInt	SNonint
02H	DFilt	FILLOFF	SMART6	SKIP6	$Yth_{(3:0)}$			
03H	$BGhfp_{(3:0)}$				$BGvfp_{(3:0)}$			
04H	$SDhfp_{(7:0)}$							
05H	$SDvfp_{(7:0)}$							
06H	$MDhfp_{(7:0)}$							
07H	$MDvfp_{(7:0)}$							
08H	$MDRedH_{(1:0)}$		$MDRedV_{(1:0)}$		$SDRedH_{(1:0)}$		$SDRedV_{(1:0)}$	
09H	$MARedH_{(1:0)}$		$MARedV_{(1:0)}$		$SARedH_{(1:0)}$		$SARedV_{(1:0)}$	
0AH	$MAhfp_{(3:0)}$				$SAhfp_{(3:0)}$			
0BH	$SAvfp_{(7:0)}$							
0CH	$MAvfp_{(7:0)}$							
0DH	$MLsel_{(3:0)}$				$SLsel_{(3:0)}$			
0EH	$MBsel_{(3:0)}$				$SBsel_{(3:0)}$			
0FH	$Bhsize_{(3:0)}$				$Bvsize_{(3:0)}$			
10H	-	SBON	$SBbrt_{(1:0)}$		-	$SBcol_{(2:0)}$		
11H	-	SBSON	$SBSbrt_{(1:0)}$		-	$SBScol2_{(2:0)}$		
12H	-	MBON	$MBbrt_{(1:0)}$		-	$MBcol_{(2:0)}$		
13H	-	MBSON	$MBSbrt_{(1:0)}$		-	$MBScol_{(2:0)}$		
14H	-	BGON	$BGbrt_{(1:0)}$		-	$BGcol_{(2:0)}$		
15H	-	-	-	SVfilt	SUVPol	SVSPol	SH_{sync}	SFPol
16H	-	-	-	MVfilt	MUVPol	MVSPol	MH_{sync}	MFPol
17H		$FBdel_{(2:0)}$			DUVPol	DVSPol	DH_{sync}	DFPol
18H	$PedestV_{(3:0)}$				$PedestU_{(3:0)}$			

If the manual mode is selected, more PiP modes become available and the I^2C bus registers 20_{HEX} to 32_{HEX} become accessible. An overview over this registers is given in Table 5 .

TABLE 5 Overview of additional I²C bus registers for manual mode

Sub Address	Data Bytes							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H	PRIO	DPal	MPal	SPal	$MVRpN_{(1:0)}$		$SVRpN_{(1:0)}$	
21H	$MHRpO3_{(1:0)}$		$MHRpO2_{(1:0)}$		$MHRpO1_{(1:0)}$		$MHRpO0_{(1:0)}$	
22H	$MHRpN3_{(1:0)}$		$MHRpN2_{(1:0)}$		$MHRpN1_{(1:0)}$		$MHRpN0_{(1:0)}$	
23H	$MHPic_{(7:0)}$							
24H	$MVPic_{(7:0)}$							
25H	$MHDis0_{(7:0)}$							
26H	$MHDis1_{(7:0)}$							
27H	$MHDis2_{(7:0)}$							
28H	$MHDis3_{(7:0)}$							
29H	$MVDis_{(7:0)}$							
2AH	$SHRpO3_{(1:0)}$		$SHRpO2_{(1:0)}$		$SHRpO1_{(1:0)}$		$SHRpO0_{(1:0)}$	
2BH	$SHRpN3_{(1:0)}$		$SHRpN2_{(1:0)}$		$SHRpN1_{(1:0)}$		$SHRpN0_{(1:0)}$	
2CH	$SHPic_{(7:0)}$							
2DH	$SVPic_{(7:0)}$							
2EH	$SHDis0_{(7:0)}$							
2FH	$SHDis1_{(7:0)}$							
30H	$SHDis2_{(7:0)}$							
31H	$SHDis3_{(7:0)}$							
32H	$SVDis_{(7:0)}$							

For a detailed description of the I2C bus registers and their effects please refer to the application notes [5] and [6].

4. Description of the PiPO - Boardset

As shown in chapter 2 there are a lot of configurations possible to implement the PiP signal processing into the video signal processing of a TV set, a VCR or a satellite receiver. In all configurations the core of the PiP signal processing is always the same. Only the frontend and backend of the PiP signal processing differs according to the flexibility and performance the user wants to have.

Following this idea, we designed an evaluation/application boardset which is modular, flexible and contains all needed blocks of the PiP signal processing.

The following Fig. 16 and Fig. 17 show the blockdiagrams of the designed application boardset and it's partitioning for two application proposals, multistandard and NTSC only.

The difference between them is only the use of the NTSC colour decoder TDA 8315T instead of the multistandard colour decoder TDA 8310A. For each colour decoder one module is designed. These modules can be mixed, if it's required. The interfaces are compatible, so the decoder modules H4VS65 and H5VS48 can be exchanged.

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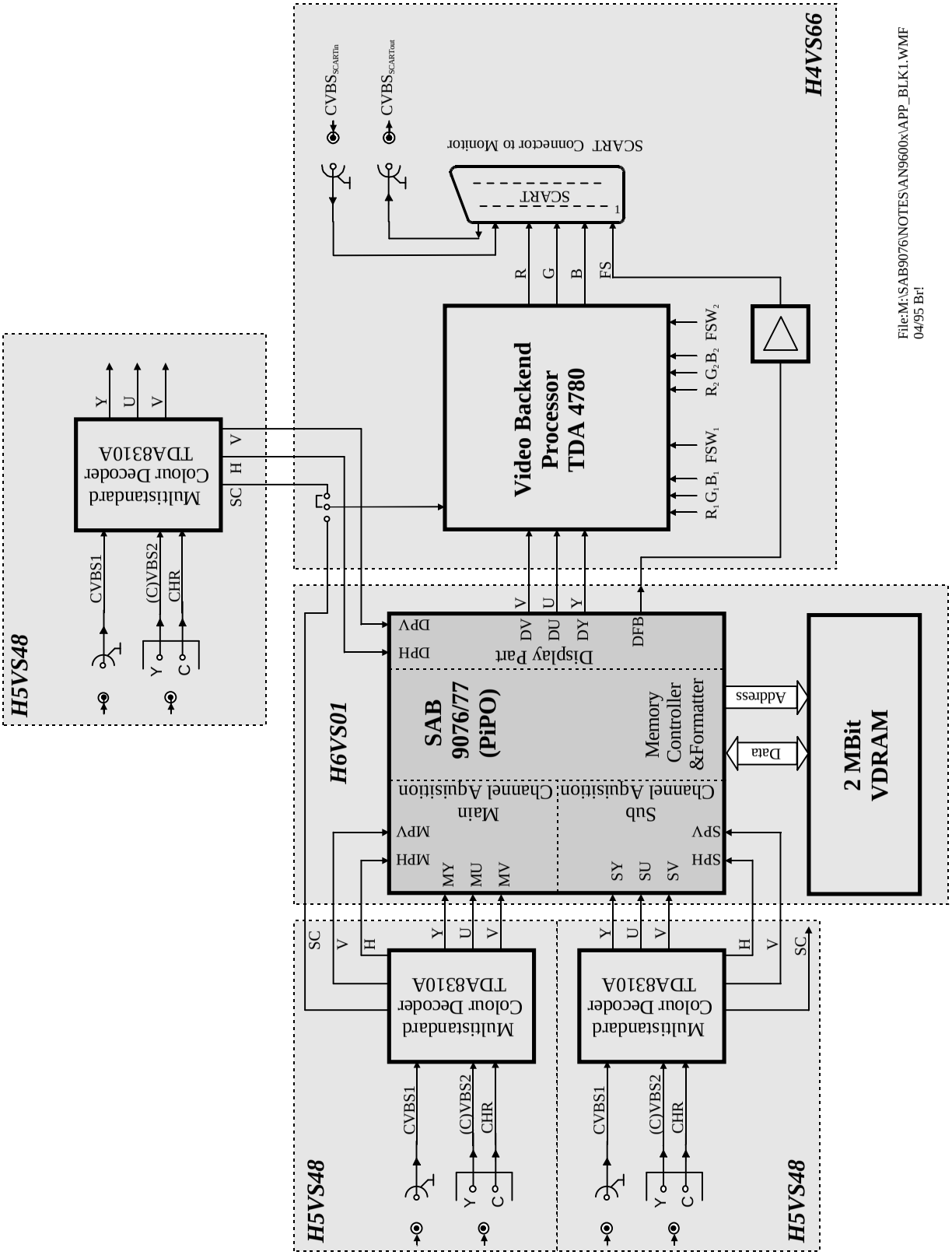

Fig.16 Partitioning of PiPO Boardset for multistandard applications

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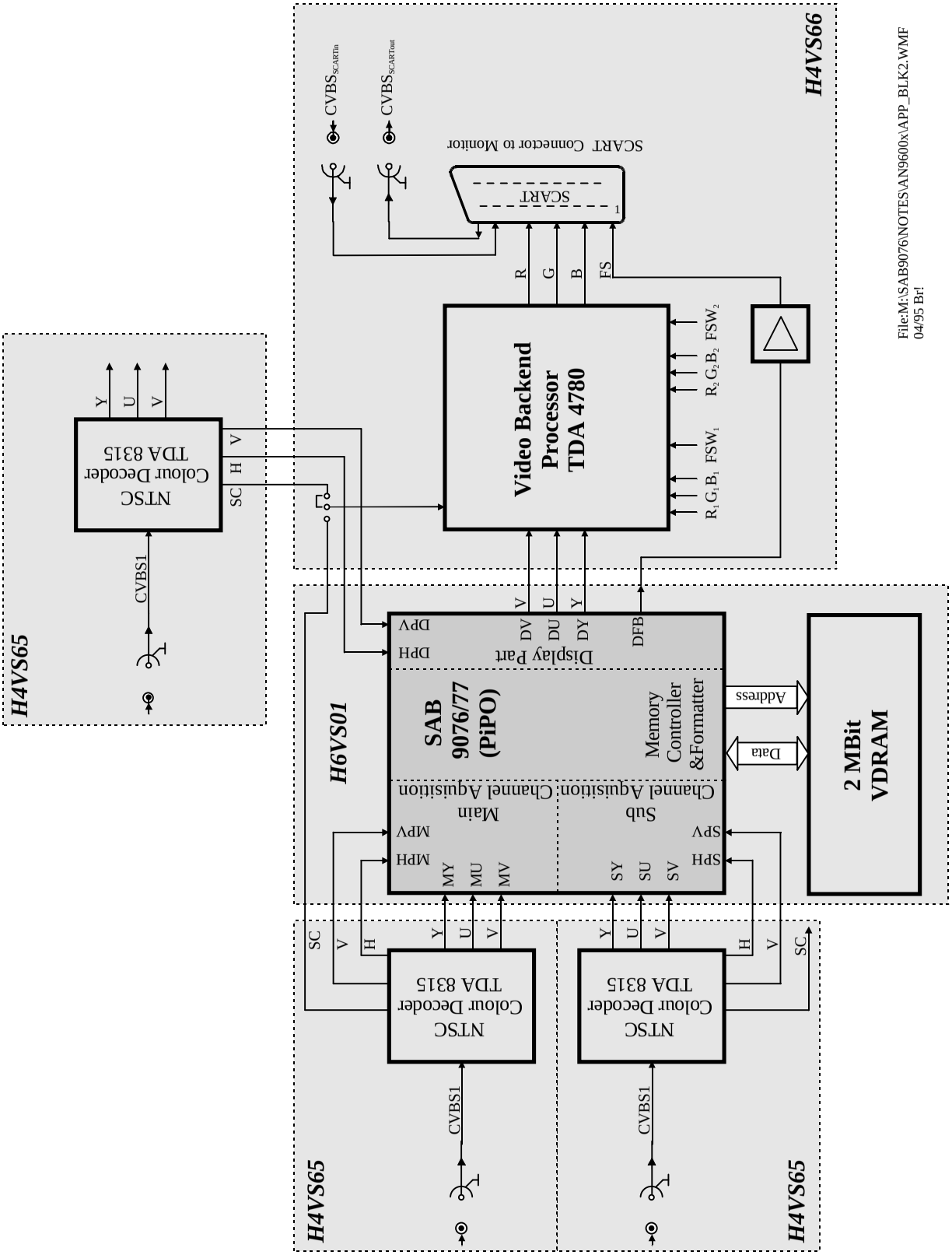


Fig.17 Partitioning of PiPO Boardset for NTSC applications

4.1 NTSC Colour Decoder Module H4VS65

4.1.1 Description of the NTSC colour decoder TDA 8315T

Detailed data about this IC are included in the Philips Semiconductors Databook IC02b “Semiconductors for Television and Video Systems”.

General description

The TDA 8315T contains a colour decoder and a sync processor. The colour decoder processes one CVBS signal or separated Y/C signals. Chroma trap- and chroma band-pass filters are included in the signal path. The trap will be switched on for CVBS inputs by grounding the chroma input pin. This is done in the application because CVBS input signals are used only. All internal filters and delays are built-up with gyrators which are fine tuned by the crystal oscillator as reference.

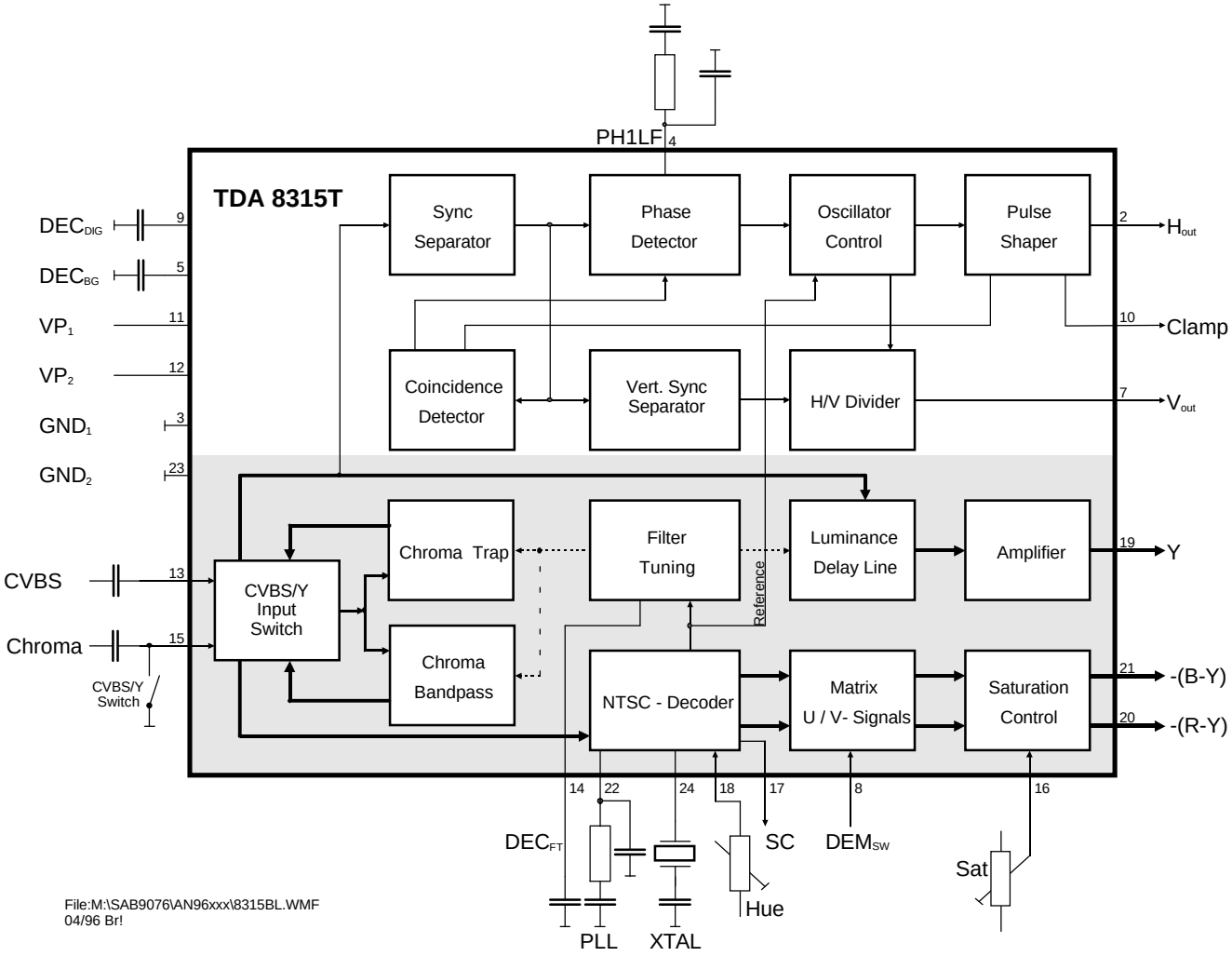


Fig.18 TDA8315: Blockdiagram of colour decoder with sync processor

Video processing path

The video processing part consists of a matrix-like CVBS/Y switch, the filters and the demodulators inside the NTSC decoder, an additional matrix for the colour difference signals, the saturation control, a delay circuit and an amplifier for the luminance path.
The decoder module H4VS65 is designed for CVBS input signals only. The chroma input (pin 15) therefore is grounded on the PCB. The incoming CVBS signal is connected via the CVBS switch to the internal chroma trap and chroma band-pass filters. These filters are aligned automatically by the filter tuning circuit.
The chroma trap reduces the chrominance of the CVBS signal by a factor of 20dB and limits the luminance bandwidth to about 2.7MHz. The luminance signal is fed back to the CVBS input switch, which supplies the luminance delay line for processing time compensation and the sync separator of the sync separation part with the luminance signal. The delay line, next block in the luminance path, is made of gyrator cells like the chroma filters. These cells are also controlled by the filter tuning circuit. The delay time for the luminance signal is 390ns. This is the internal processing time for the chrominance signal to be demodulated. The delay between CVBS input signal and luminance output signal is about 516 ns.The last stage in the luminance path is an amplifier with an output impedance of 390 Ohms. The complete processed luminance signal is available at pin 19 and has an amplitude of 1.5 V black to white using a standard CVBS signal.
The bandwidth of the luminance channel is 2.7 MHz at -3 dB. This is well adapted to the PIP environment.

The chroma bandpass filter separates the chrominance signal out of the CVBS signal and supplies it to the NTSC decoder via the CVBS input switch. The chroma bandpass filter is designed using gyrator cells, which are controlled by the filter tuning circuit. An automatic gain control for the chrominance output signal is included.
The NTSC decoder part consists of an alignment free crystal oscillator, a phase shifting stage, a subcarrier amplifier and two demodulators.
The crystal oscillator operates on 1* f_{SC} and needs only one crystal and a network for the internal loop filter. Two types of crystals can be used:

1. Unique NTSC crystal with f = 3.579 545 MHz (12NC 9922 520 00412). This crystal needs a serial load capacitor of 18pF.
2. Special NTSC crystal with f = 3.579 545 MHz (12NC 9922 520 00382). This crystal is designed for the colour
   decoder of the TDA83xx series and needs no serial load capacitor.

The network for the internal loop filter is a combination of a resistor of 100kΩ in line with a capacitor of 100nF, all in parallel to a capacitor of 4.7nF.
The oscillator delivers the reference frequency to the filter tuning circuit, the phase shifting stage, the output amplifier and to the line oscillator of the sync processing part. The amplifier gains the subcarrier signal to an amplitude of 300mV pp and provides it with an output impedance of 250 Ohms at pin 17. The subcarrier output signal isn't further used on the decoder module H4VS65.
The phase shifting stage generates two subcarrier signals with a phase difference of 90° for the demodulators. The carrier with a phase of 0° in respect to the subcarrier burst of the incoming CVBS signal is fed to the U-demodulator and the carrier with a phase of 90° is fed respectively to the V-demodulator. The phase shift between the two carriers is fixed, but the phase relationship between the demodulator carriers and the burst phase of the incoming CVBS signal can be varied by the HUE control voltage, applied to pin 18. This allows the variation of the HUE control of ± 45 º, see Fig. 19 .

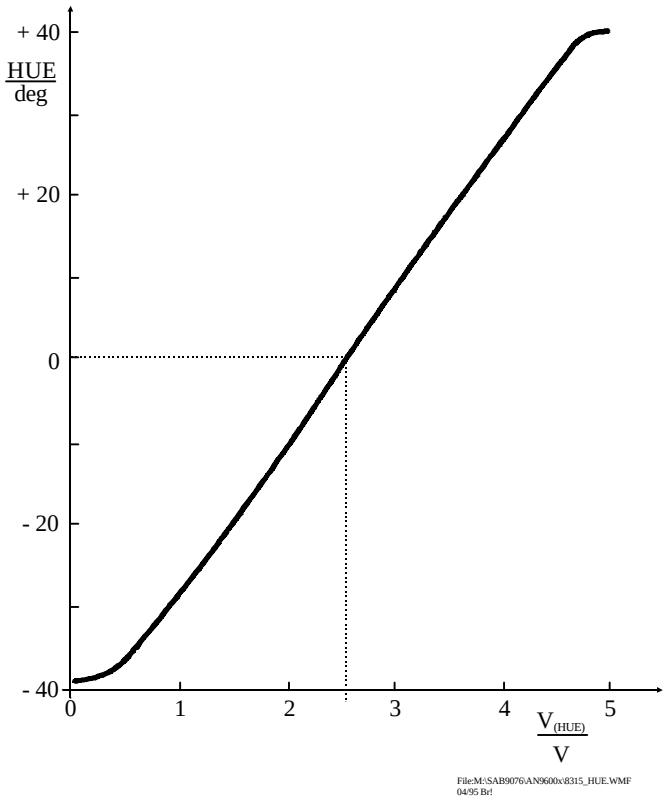


Fig.19 HUE Control curve for TDA 8315T

The demodulators have the same gain. The output signals of the demodulators are the baseband colour difference signals U and V [U and V are the amplitude-scaled colour difference signals (B-Y) and (R-Y) respectively]. Together with a HUE of -5° this is due to the Japanese standard.

These signals are fed to an internal matrix, which changes the demodulation angle for the colour difference signal V from 90° to 110°, if the control voltage of pin 8 (DEM_{SW}) is $V_{(DEMSW)} > 1$ V. The case of 90° demodulation angle meets the Japan NTSC standard while the 110° case meets the US-NTSC standard. The input pin 8 has no internal pull-up or pull-down resistor. It should be connected to the appropriate voltage to ensure correct matrizing.

The normal output swing of the inverted colour difference signals -(R-Y) and -(B-Y) will be 1.5 Vpp at 90° demodulation angle for a FCC standard colour bar signal. At 110° demodulation angle the -(R-Y) component will be reduced to 1.2 Vpp. With the external HUE control voltage at pin 18 the demodulation angle can be fine tuned.

The last stage in the chroma path is a voltage controlled amplifier. The output amplitude of the colour difference signals (saturation) can be controlled over a range of 54 dB by the voltage SAT at Pin 16 as shown in Fig. 20 .

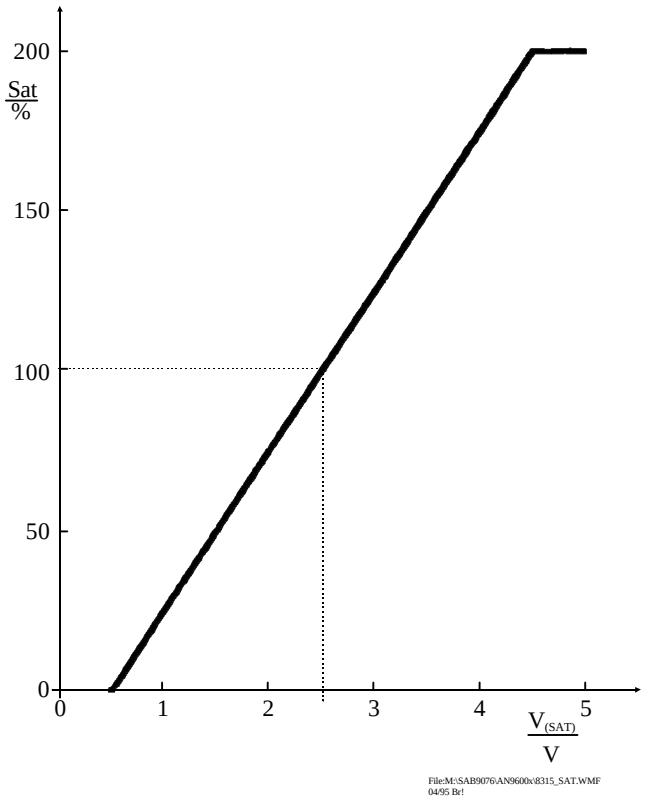


Fig.20 SAT Control curve for TDA 8315T

The overall bandwidth of the chroma signal path is 0.65 MHz at -3 dB.
The colour difference signals -(B-Y) and -(R-Y) have an equal signal swing of 1.5 Vpp at a FCC standard colour bar signal and 90° demodulation angle. This simplifies the ADC input interfacing with the PiP controller SAB 9076/77 and improves the signal to noise ratios.

The internal band gap reference should be decoupled at pin 5 by two capacitors of 1 µF and 22 nF. The capacitance should not exceed 1.1 µF.

Sync pulse generation

The sync separator amplifies the sync pulses and slices at a 70% level for strong signals and 30% level for weak signals. A controlled phase detector with an external loop filter feeds to the internal oscillator and the coincidence detector. The coincidence detector observes, if the H-PLL is sychronized with the sync pulses of the incoming CVBS signal. The oscillator is running on the double line frequency to obtain an accurate duty cycle of 50% for the following pulse shaper. The pulse shaper contains a circuitry to form and buffer the outgoing pulses H_{out} and Clamp as well as a reference pulse for the coincidence detector.
Without input signal, the PLL is working on a free running frequency which is referenced to the crystal oscillator. This results in an offset less 2% to the line frequency.

Two types of horizontal sync pulses are provided. The H_{out} pulse with a width of t_W = 5.4 µs and a Clamp pulse (t_W = 3.4 µs) at the back porch.
The H_{out} pulse starts with the falling edge of the sync part of the incoming CVBS signal.The H_{out} pulse is available at pin 2 and has an output impedance of 2 kΩ.

The Clamp pulse starts with the trailing edge of the H_{out} pulse and covers the burst pulse location on the back porch.The Clamp pulse is available at pin 10 and has an output impedance of 2 kΩ

The vertical sync pulse is generated by a count-down circuitry and genlocked to a pulse which is separated from the sliced sync signal by the vertical sync separator. The pulse has a width of t_W= 380 µs and starts with the falling edge of the H pulse or half a line later, depending on the field. The Vout -pulse is available at pin 7and has an output impedance of 2 kΩ.

Because the H-oscillator is still running in a free running mode when no CVBS input signal is available and because the V_{out} pulse is generated by a counter out of the H pulses, it is insured that H_{out}, Clamp and V_{out} pulses are always available, even when no input signal is applied to the device.

For the PIP module only the burst key-like Clamp pulse and the vertical sync signal are used as horizontal and vertical references. The exact timing is shown in Fig. 21 .

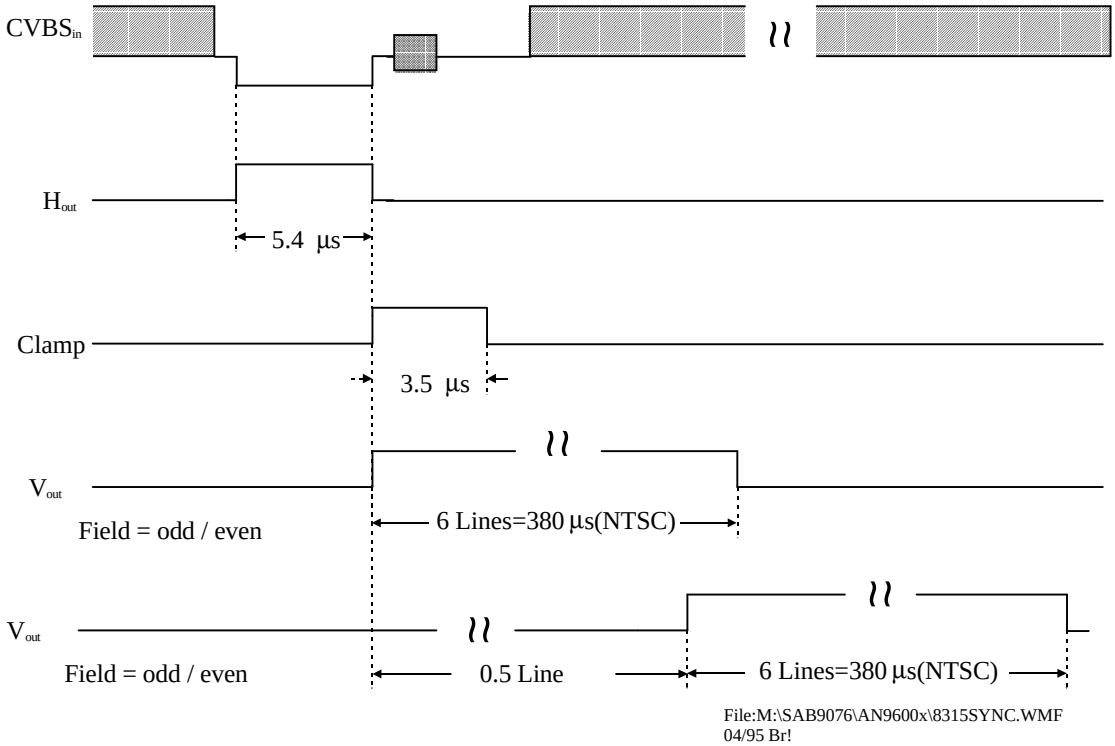


Fig.21 TDA8315: Timing of generated sync signals

The Phi1 loop filter should have a time constant of 12 ms. This can be realized by a 12kΩ resistor and 1 µF capacitor. In parallel a small capacitor of 4.7nF should be used for integrating high frequency components.

The supply pins 11 and 12 can be tied together. They should be properly decoupled by 47 nF in parallel with 47 µF capacitors.

4.1.2 Description of the decoder module H4VS65

The schematics of the NTSC decoder module H4VS65 is shown in Fig. 22 .

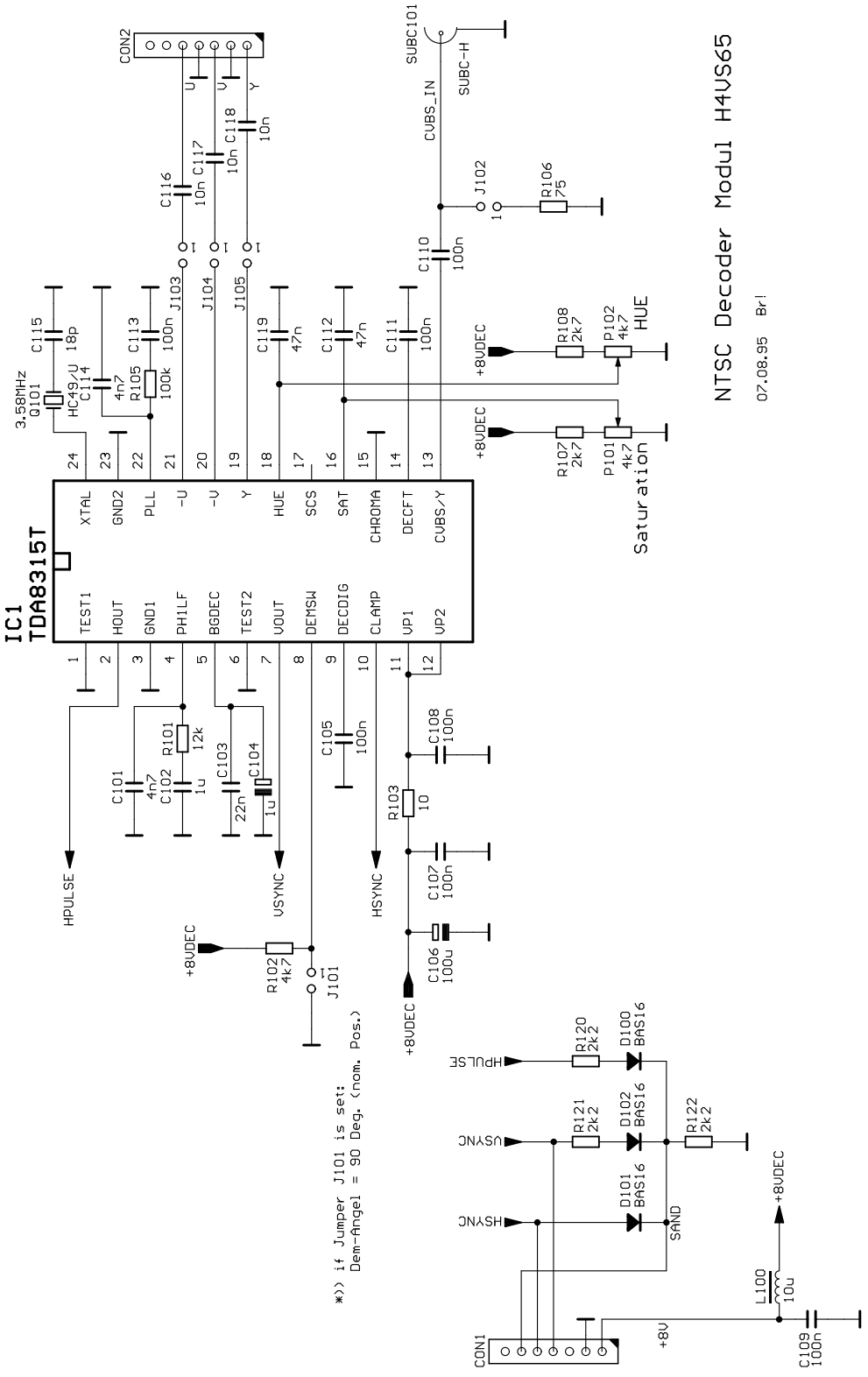


Fig.22 Schematics of NTSC decoder module H4VS65

Inputs

The CVBS input signal is connected to the PCB via a SUBCLIC connector and coupled with a 100 nF capacitor to pin 13 (CVBS/Y) of the IC. The input is terminated with 75Ω if jumper J102 is set. This configuration allows the module to be connected to a token ring system without a termination of the incoming CVBS signal.

The second input of the IC (pin 15, CHROMA) has to be grounded, because the PCB isn't designed to handle SVHS signals.

Outputs

The IC provides the output signals Y, -(R-Y), -(B-Y) at the pins 19 (Y), pin 20 -(R-Y) and pin 21 -(B-Y). The signals are connected via the jumpers J105, J104 and J103 and the coupling capacitors C118, 117, 116 = 100nF to connector CON 2. The jumper are used to open the video signals pathes for measuring purposes. The coupling capacitors are needed, if the PCB is connected to other applications. **In our PiP Boardset the coupling capacitors are placed on the PiP main module. For that reason the coupling capacitors are replaced by 0Ω resistors.**

The pulses for synchronisation H_{out}, V_{out} and Clamp are available at the pins 2 (H_{out}), pin 7 (V_{out}) and pin 10 (Clamp).
The pulses H_{out} and V_{out} are directly connected to the pin 4 (VSync) and pin 5 (HSync) of connector CON1. Both pulse together with the Clamp pulse are combined to a quasi sandcastle signal. The combination of the three signals and the matching of their amplitudes is realized by a simple diode/resistor network. The sandcastle signal is available on pin 6 of connector CON1 and is used for synchronizing the video processor TDA 4780.
For testing the synchronisation pulses the connector pins should be probed directly.

IC controls

The input selection switch SVHS/CVBS (pin 15) is described above. Applying an DC voltage $V_{pin15} < 1V$ set the input switching matrix of the IC into CVBS mode. That means, that all internal filters are activated and the chroma input is disabled. Exceeds the applied voltage $V_{pin15} > 3V$ the matrix is switched to SVHS mode. That means, that the internal filters are disabled and the chroma input is activated. No internal pull-up or pull-down resistors are included, so an unconnected pin 15 should be avoided.

The applied voltage at pin 8 (DEMSW) sets the demodulation angle between the U- and V axis.Because this input misses the pull-up or pull-down resistors too, an unconnected pin 8 should be also avoided.
If the voltage is lower than 1V, the demodulation angle is 90° and conform with the japan NTSC standard. For switching the device to a demodulation angle of 110° to be conform with the US NTSC standard, the applied voltage has to be at least V_{Supply} - 1V.
On the PCB the switching is realized by the combination of pull-up resistor R102 and jumper J101.

TABLE 6 Demodulator Angle Setting by Jumper J101

Jumper J101	$V_{pin\,8}$	Dem - Angle	Standard	Amplitude		
				(R-Y)	(B-Y)	Y
set	0 V	90 °	Jp-NTSC	1.5 V_{pp}	1.5 V_{pp}	1.5 V_{pp}
not set	8 V	110 °	US-NTSC	1.5 V_{pp}	1.2 V_{pp}	1.5 V_{pp}

By default the jumper J101 is set on the PCB to make the best use of the permissible input voltage swing of the PiP controller. The Jp-NTSC standard is chosen. If an adaption to the US-NTSC standard is desired, the different matrixing can be done by the video processor TDA 4780.

The adjustment of saturation and HUE of the IC are obtained by two DC voltages, referenced to the control

curves shown in Fig. 19 and Fig. 20 . On the module H4VS65 the control voltage is derived from the 8V supply via a series resistor of 2.7 kΩ and a potentiometer of 4.7 kΩ to ground. The derived control voltages are lead to pin 16 (SAT) and pin 18 (HUE) of the IC. Each of these pins is decoupled with a 47nF capacitor to ground to removed any noise on the control voltages and to avoid the modulation of the saturation or HUE by low frequency noise.

Loop Filters

For the loop filter of the line oscillator, connected to pin 4 (PH1LF), a serial combination of a 12 kΩ resistor and a 1µF capacitor, together with a 4.7nF capacitor in parallel to ground are used.
For the loop filter of the subcarrier oscillator, connected to pin 22 (PLL), we recommend a series combination of a 100 kΩ resistor and a 100 nF capacitor, together with a 4.7nF capacitor in parallel to ground.
This configuration gives the best results in case of phase stability in locked condition and in case of lock-in behaviour.

Crystal

The reference element for the subcarrier oscillator is a normal NTSC crystal (f_0 = 3.579 545 MHz) [12NC9922 520 00412]. **This crystal needs a serial load capacitor of 18pF.**

Decoupling

The IC has it's own bandgap reference, to generate all bias currents and reference voltages, which are internally needed. To protect this major internal node from noise, it has to be decoupled externally by a parallel combination of an electrolytic capacitor of 1µF and a capacitor of 22nF. This combination is connected to pin 5 (BGDEC) of the IC and should be grounded to a "quiet" ground potential.

The internal supply rail for the digital part of the IC should be decoupled with a 100nF capacitor, connected to pin 9 (DECDIG).

The circuitry for the internal filter tuning needs to be decoupled to obtain the filter adjustment with a good performance. For this, a capacitor of 100nF is connected to pin 14 (DECFT) of the IC. The capacitor should be connected to a "quiet" ground potential, too.

Supply

The two supply pins 11 and 12 of the IC can be tied together. The proposed decoupling combination shown on the schematics is optimized to fulfil two major conditions:

1. The distortions, generated by the IC itself should be kept as internal as possible and shouldn't be emitted on the supply system.
2. The distortions in the supply system, especially due to long supply lines, shouldn't reach the supply pins of the IC.

The chosen application is thought to meet the requirements of the PiP Boardset. For applications of the TDA8315T in other environments, the decoupling combination can be different.

4.1.3 Interface and Probing

The following Fig. 23 shows the placement of all major elements for adjusting or setting the IC as well as the location of the most interesting output signals of the PCB.
Table 7 lists the relevant data of the signals on the interface connectors.

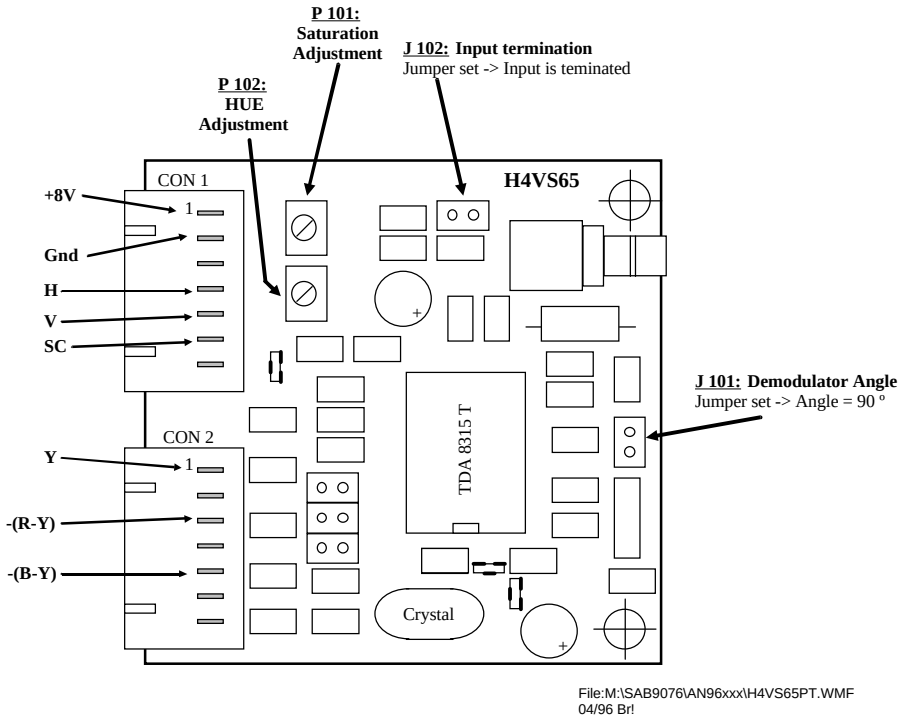


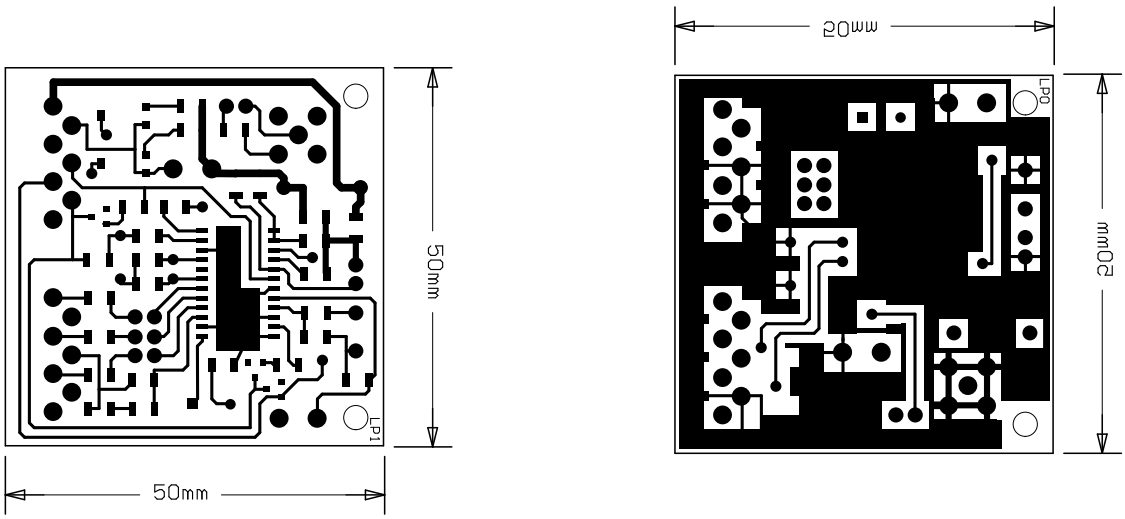
Fig.23 Relevant signals, settings and adjustments of H4VS65

TABLE 7 Characteristics of Interface-signals

Cond.: 100/75 NTSC Standard Colour Bar Testsignal; Supply = 8V						
Signal-name	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
$CVBS_{in}$	1.0 Vpp*	-	-	-	63.55 µs	Video: 700 mVpp Sync : 300 mVpp any DC-Level Input termination: 75 Ω
Y	1.5 Vpp*	2.92 V	5.20 V	-	63.55 µs	Black-Level = 3.5 V_{DC}
-(B-Y)	1.5 Vpp*	2.34 V	3.90 V	-	63.55 µs	no-colour-Level = 3.2 V_{DC}
-(R-Y)	1.5 Vpp*	2.36 V	3.90 V		63.55 µs	no-colour-Level = 3.2 V_{DC}
H	4.5 Vpp	0 V	4.5 V	3.4 µs	63.55 µs	-
V	5.0 Vpp	0 V	5.0 V	380 µs	16.68 ms	-
SC	3.8 Vpp	0 V	3.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 380 µs	63.55 µs	Burst-Key-Top = 3.8 V_{DC} H-Pulse-Top = 2.12 V_{DC} H-Pulse-Top during V = 2.9 V_{DC} V-Pulse-Top = 2.12 V_{DC}
+8V	-	-	-	-	-	Supply Voltage
***) = Demodulation Angle = 90° ~> Jumper J101 is set**						

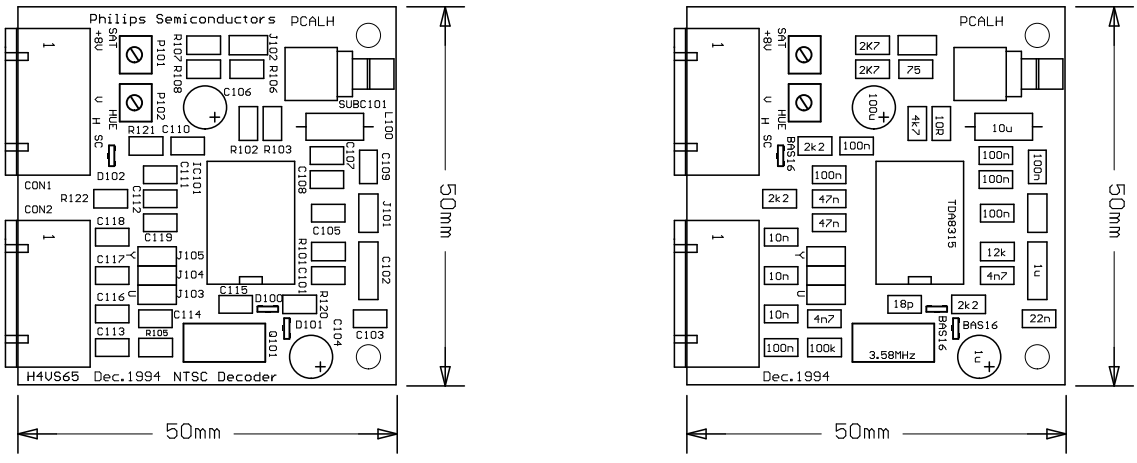
4.1.4 Layout and Placement

The following figures show the layout and placement for H4VS65 in original scale.



Layout of Topside | Layout of Bottomside

Fig.24 Layout of NTSC-Decoder module H4VS65



Placement of Topside-Components | Values of Topside-Components

Fig.25 Components of NTSC-Decoder module H4VS65

No special application hints for the layout have to be observed for implementation of the NTSC-colour decoder circuitry in an environmental PCB layout.

4.2 Multistandard Decoder TDA 8310A on H5VS48

The multistandard colour decoder module H5VS48 contains the multistandard colour decoder IC TDA 8310A, the SECAM decoder IC TDA 8395, the baseband delay line TDA 4665T and some additional circuitry to obtain the required interface signal quality.

4.2.1 Description of TDA 8310A

Detailed data about this IC you will find in the Philips Semiconductors Databook IC02b [1] and in the data sheet [2].

General description

The TDA 8310A is a multistandard colour decoder and sync processor out of the TDA83xx-family. The IC is a derivative of the TDA 8310. The IF section of the TDA 8310 has been omitted.
The decoder processes two CVBS input signals or one separated Y/C input signal. Chroma trap and chroma band-pass filter are included in the signal path. The filters will be activated by a switching voltage applied via one pin or by an automatic detection circuit. All internal filters are built-up with gyrators which are fine tuned by the crystal oscillator as reference.

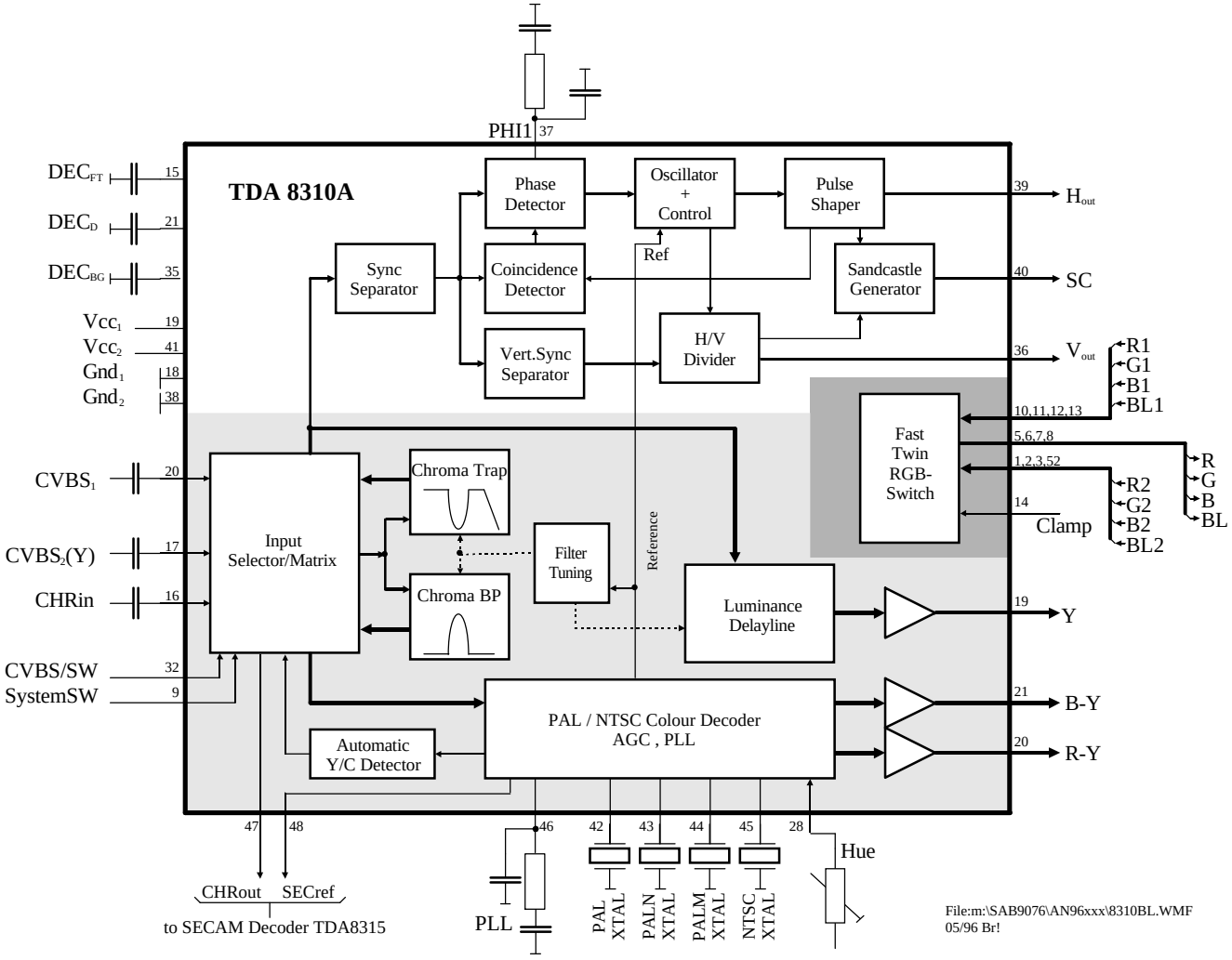


Fig.26 Blockdiagram of multistandard colour decoder TDA 8310A

Video processing path

The video processing path consists of an input selector and signal path matrix, the filters, the demodulators and oscillators inside the multistandard colour decoder, a delay circuit and buffer/amplifier for all three signal outputs. The decoder module H5VS48 is designed to handle CVBS- and Y/C input signals. So the flexibility, the TDA 8310A offers, is used in the actual application.
The IC has two CVBS inputs $CVBS_1$ (pin 20) and $CVBS_2$/Y (pin 17). The selection between the CVBS input signals is arranged by the external switching voltage CVBS/SW, connected to pin 32. The second CVBS input is simultaneously the luminance input, when the IC is switched into the Y/C mode. The mode selection is arranged by the external switching voltage SystemSW, connected to pin 9, or by the automatic Y/C detector. The external switching voltage at pin 9 overrules the output voltage of the automatic Y/C detector.
Depending on the applied switching voltages the selected input signal is fed to the chroma trap and the chroma band-pass filter simultaneously. The filters are aligned automatically by the filter tuning circuit.
The chroma trap reduces the chrominance signal of the selected CVBS signal at least by a factor of 20 dB and limits the luminance bandwidth to about 3.5 MHz, if PAL standard is selected. The luminance signal is fed back to the input selector/matrix, which supplies the luminance delay line and the sync separator of the sync separator part. The luminance delay line, the next block in the luminance path, is made of gyrator cells like the filters and is controlled by the same filter tuning circuit. The delay time for the luminance signal is 390 ns. This is the internal processing time for the chrominance signal to be demodulated. The last stage in the luminance path is an amplifier/buffer with an output impedance of typical 100 Ω. The complete processed luminance signal is available at pin 49 and has an amplitude of 1.0 V black to white using a standard CVBS signal. The delay between CVBS input signal and luminance output signal is about 470 ns independent of the standard of the applied CVBS input signal.
The bandwidth of the luminance channel is 2.9 MHz for NTSC and 3.5 MHz for PAL at -3dB. This is well adapted to the PiP environment.

The chroma band-pass filter separates the chrominance signal out of the selected CVBS signal and supplies it to the PAL/NTSC demodulator via the input selector/matrix. At the same time the chrominance signal is fed to the pin 47 (CHRout) to be connected to the SECAM add-on colour decoder TDA 8395. The chroma bandpass filter is designed using gyrator cells, which are controlled by the filter tuning circuit. If the Y/C mode is selected, the chroma trap and chroma band-pass filter are bypassed and the input signals are directly fed to the matrix outputs belonging to them.
The colour decoder consists of an automatic gain control, an alignment-free crystal oscillator, a phase shifting stage, the demodulators, a colour standard identification stage, a subcarrier amplifier and control logic.

The subcarrier oscillator operates on 1* f_{SC} and needs four different crystals to cover all colour standards used in the world.These crystals are directly connected to the pins XTAL/P (pin 42) for PAL/BG, to XTAL/PN (pin 43) for PAL/N, to XTAL/PM (pin 44) for PAL/M and to XTAL/M (pin 45) for NTSC/M. Two different classes of crystals can be used, see Table 8 .

TABLE 8 Crystals for Multistandard Colour Decoder TDA 8310A

Condition	Colour Standard	Frequency	12NC - Code
Application with serial load capacitor	PAL / BG	4.433619 MHz	4322 143 04043
	PAL / N	3.582056 MHz	9922 520 00411
	PAL / M	3.575611 MHz	9922 520 00413
	NTSC / M	3.579545 MHz	9922 520 00412
Application without serial load capacitor	PAL / BG	4.433619 MHz	9922 520 00384
	PAL / N	3.582056 MHz	9922 520 00381
	PAL / M	3.575611 MHz	9922 520 00383
	NTSC / M	3.579545 MHz	9922 520 00382

The network for the internal loop filter is a combination of a resistor of 100 kΩ in line with a capacitor of 100 nF, all in parallel to a capacitor of 4.7 nF.
The oscillator delivers the reference frequency to the filter tuning circuit, the phase shifting stage and the output amplifier as well as to the line oscillator of the sync processor part. The amplifier gains the subcarrier signal to an amplitude of 250mV typical and provides it at pin SECREF (pin 48) as reference for the SECAM add-on colour decoder TDA 8395. The signal is only available, if the crystal for PAL/BG is selected. For PAL/BG the subcarrier reference signal is continuously provided. For SECAM, when the same crystal is used, the subcarrier reference signal is gated and only available during vertical blanking. If one of the other or no colour standard is identified, the reference signal at pin 48 is blanked.
The subcarrier reference signal at pin 48 is combined with a DC voltage, which is depending on the recognized colour standard. Only if SECAM is identified, the DC voltage is above 4.3 V, otherwise below 1.7V [for more informations see under 4.2.2 “Handshake communication between TDA 8310A and TDA 8395”] .

The phase shifting stage generates two subcarrier signals with a phase difference of 90° for the demodulators. The carrier with a phase of 0° in respect to the subcarrier burst of the incoming CVBS signal is fed to the U-demodulator and the carrier with a phase of 90° is fed respectively to the V-demodulator. The phase shift between the two carriers is fixed, but the phase relationship between the demodulator carriers and the burst phase of the incoming CVBS signal can be varied by the HUE control voltage, applied to pin 28, if NTSC M colour standard is identified. The variation of the HUE control is ± 45 º, see Fig. 27 .

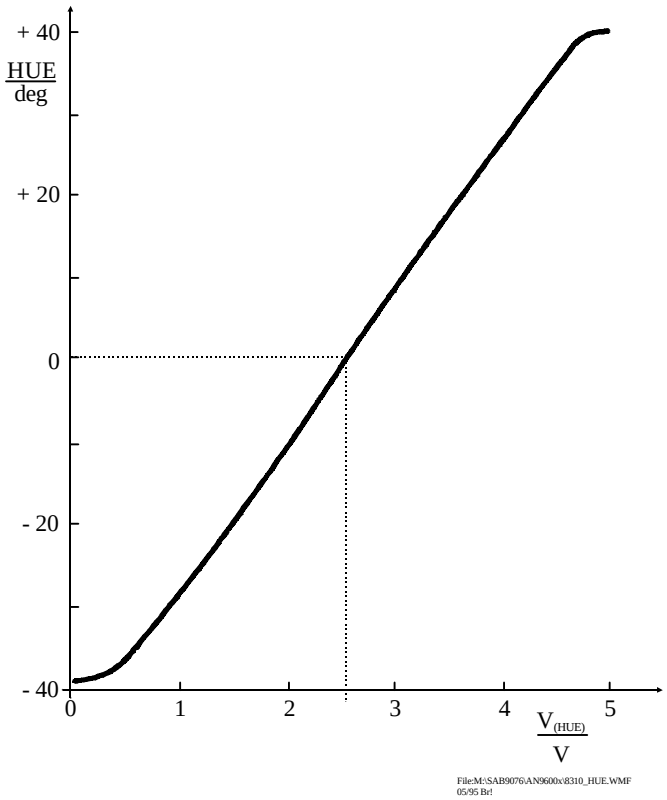


Fig.27 HUE control curve for TDA 8310A

The demodulators have the same gain. The output signals of the demodulators are the baseband colour difference signals -(R-Y) and -(B-Y), which are fed to output amplifiers/buffers with fixed gain. A saturation control function is obsolete, because the colour decoder part contains an AGC circuit, which controls the amplitude of the chrominance signal in reference to the burst amplitude of the incoming CVBS signal.
The -(B-Y) and -(R-Y) signals are provided at the pins B-Y (pin 21) and R-Y (pin 20). The signal swing is 1.05Vpp for -(R-Y) and 1.33Vpp for -(B-Y) for a standard CVBS colour bar test signal. The overall bandwidth of the chroma path is 0.65 MHz at -3dB.
The output amplifier/buffer provide the output signal with an output impedance of 500 Ω max. In case of SECAM they are switched into highohmig threestate mode [for more informations see under 4.2.2 “Handshake communication between TDA 8310A and TDA 8395”].

The colour decoder part provides four lines to indicate which colour standard is identified and which crystal is used. These lines are directly connected to the pins XTAL/L2 (pin 23), XTAL/L1 (pin 24), CSL2 (pin 25) and CSL1 (pin 26). These pins are bidirectional inputs/outputs and operate as indication pins as well as control pins to force the colour decoder part into a wanted colour standard mode.

The signal processing path contains the bandgap reference circuit, which should be decoupled at pin DECBG (pin 35) by two capacitors of 10µF and 100nF in parallel. The filter tuning circuit needs the same combination for decoupling at the pin DEC (pin 15).

RGB - Multiplexer

The TDA 8310A provides a fast multiplexer (switch) for two sets of RGB signals incl. their fast blank signal. The RGB multiplexer is completely independent of the other IC-parts.
The RGB multiplexer can handle input signals with an amplitude of 1.3Vpp max. The input impedance is at least 100 kΩ for the RGB inputs.
The selection of the RGB input signals to be connected to the output is arranged by the blank input signals of the associated channels. A high level at BLIN1 (pin 13) leads the set of $(RGB)_1$ to the RGB outputs and BLOUT (pin 5) gets high level. A high level at BLIN2 (pin 52) connects the set of $(RGB)_2$ to the RGB outputs and BLOUT (pin 5) gets high level. The blank pulse BLIN2 and its appropriate $(RGB)_2$ signals have priority.
The clamp pulse, connected to pin 14, serves the clamping of the RGB input to an internal reference voltage.
If BLIN1 and BLIN2 are both low, the RGB outputs and the blank output are switched into high impedance state, so that other switches can be used in parallel. In threestate the output impedance is at least 100 kΩ.
If active, the RGB outputs offer the selected set of RGB input signals with an output impedance of 150 Ω max and the blank output has an output impedance of 300 Ω max.

Sync pulse generation

The sync separator amplifies the sync pulses and slices at a 70% level for strong signals and 30% level for weak signals. A controlled phase detector with an external loop filter feeds to the internal oscillator and the coincidence detector. The coincidence detector observes, if the H-PLL is sychronized with the sync pulses of the incoming CVBS signal. The oscillator is running on the double line frequency to obtain an accurate duty cycle of 50% for the following pulse shaper. The pulse shaper contains a circuitry to form and buffer the outgoing pulses HS as well as a reference pulse for the coincidence detector.
Without input signal, the PLL is working on a free running frequency which is referenced to the crystal oscillator. This results in an offset less 2% to the line frequency.

Two types of horizontal sync pulses are provided. The HS pulse with a width of t_W= 5.4 µs and a Sandcastle pulse.
The HS pulse starts with the falling edge of the sync part of the incoming CVBS signal.The HS-pulse is available at HS (pin 39) and has an output impedance of 2 kΩ.
The Sandcastle pulse starts with the trailing edge of the HS pulse with the H-level, arises to the burstkey top with the beginning burst pulse and falls back after 3.5 µs.The Sandcastle pulse has a pulse width of 8.9 µs. During vertical blanking the sandcastle signal has continuously H-level with added brustkey pulses.
The Sandcastle pulse is available at SC (pin 40) and has an output impedance of 2 kΩ.

The vertical sync pulse is generated by a count-down circuitry and genlocked to a pulse which is separated from the sliced sync signal by the vertical sync separator. The pulse has a width of t_W= 380 µs respectively 6 lines for NTSC/M or t_W= 320 µs respectively 5 lines for PAL/SECAM and starts with the falling edge of the HS pulse or half a line later, depending on the field. The delay time between start V pulse of the incoming CVBS signal and start of the VS pulse at pin VS is typically 37.8 µs.The VS pulse is available at VS (pin 36) and has an output impedance of 2 kΩ.

Because the H-oscillator is still running in a free running mode when no CVBS input signal is available and because the VS pulse is generated by a counter out of the H pulses, it is ensured that HS, SC and VS pulses are always available, even when no input signal is applied to the device.

For the PIP module only the horizontal sync pulse and the vertical sync signal are used as horizontal and vertical references. The exact timing is shown in Fig. 28 .

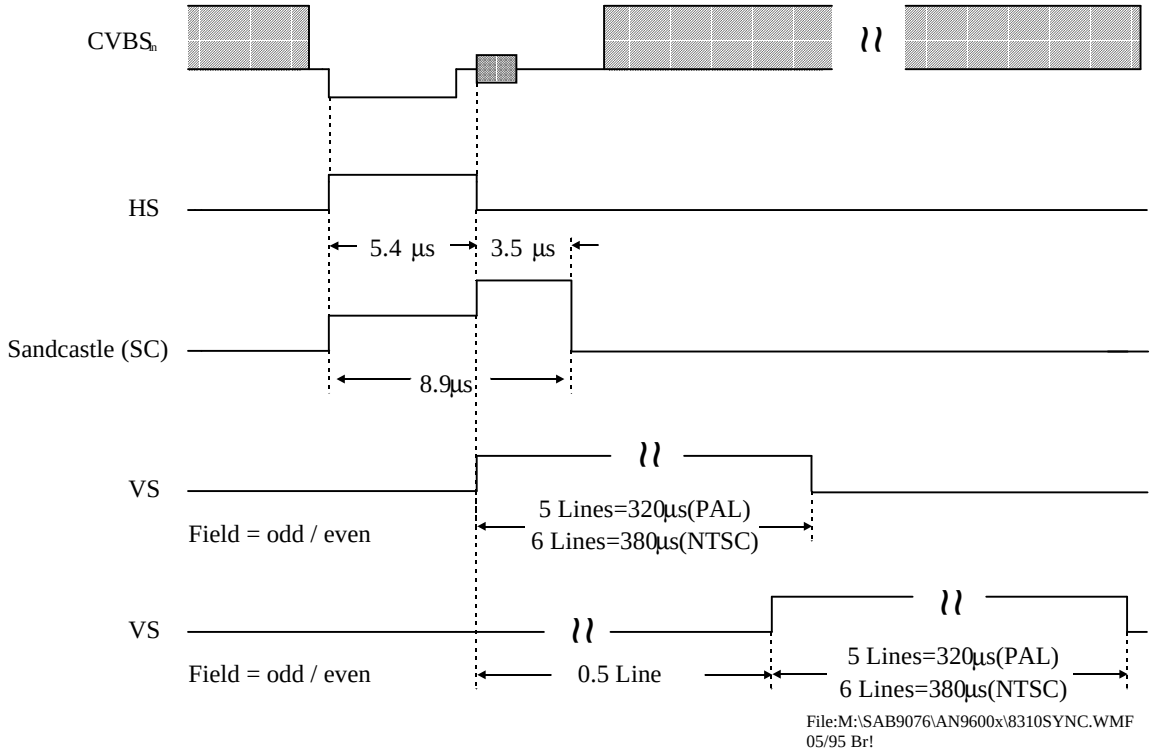


Fig.28 TDA8310A: Timing of generated sync signals

The Phi1 loop filter should have a time constant of 12 ms. This can be realized by a 12kΩ resistor and 1 µF capacitor. In parallel a small capacitor of 4.7nF should be used for integrating high frequency components.

4.2.2 Description of the multistandard decoder module H5VS48

The conception of the multistandard colour decoder module H5VS48 is shown in the blockdiagram of Fig. 29 . The module contains the multistandard decoder IC TDA 8310A, the SECAM add-on colour decoder TDA 8395 and the baseband delayline TDA 4665T as well as three amplifiers to adapt the output amplitude of the ICs to the required levels for the PiP controller inputs.

The schematics are drawn on three sheets, shown on Fig. 30 , Fig. 31 and Fig. 32 . The partitioning is:

Sheet 1: TDA 8310A, application and environment
Sheet 2: SECAM decoder TDA 8395 and baseband delayline TDA 4665T
Sheet 3: Amplifiers and Interfacing

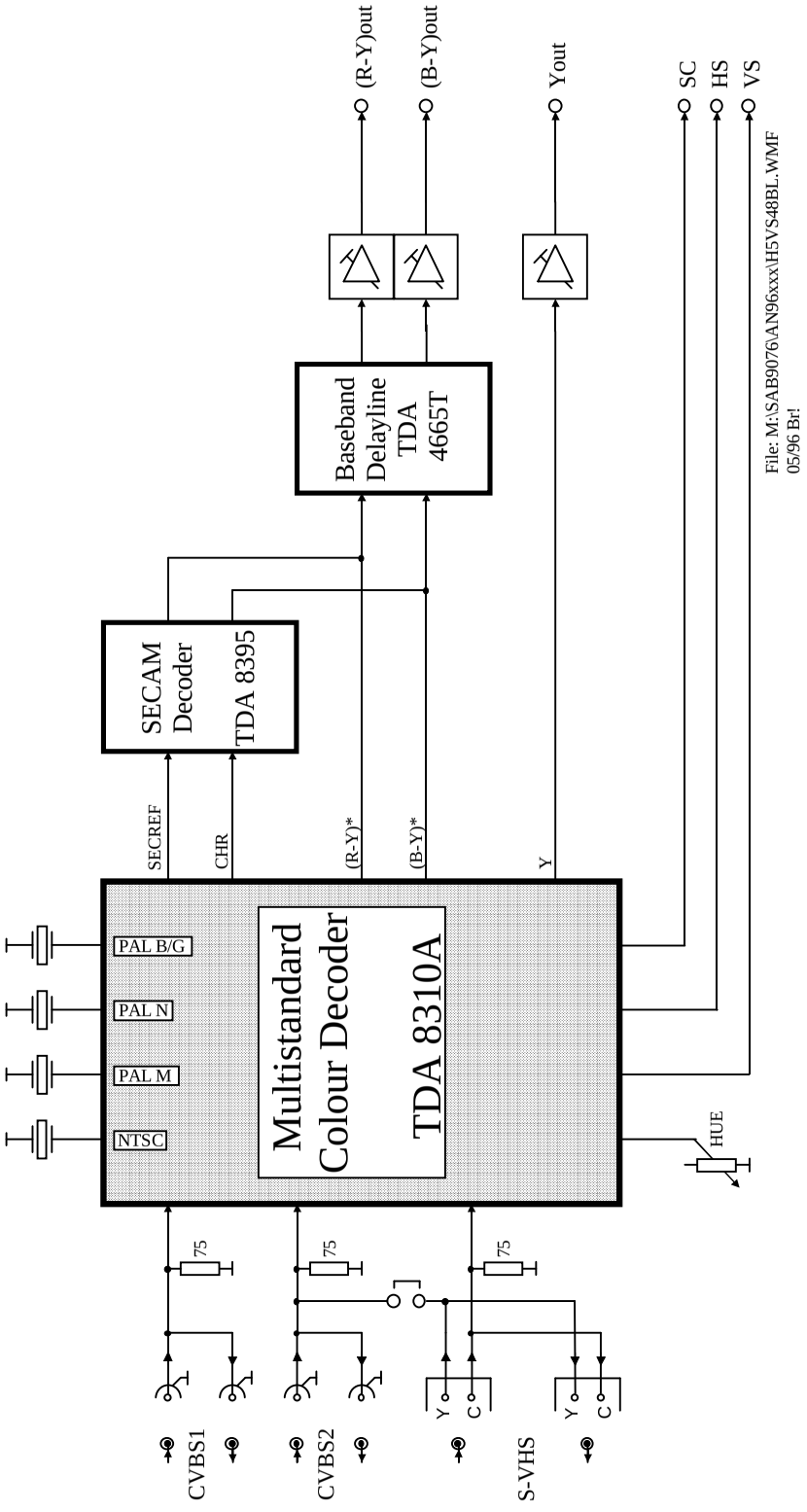


Fig.29 Blockdiagram of multistandard colour decoder module H5VS48

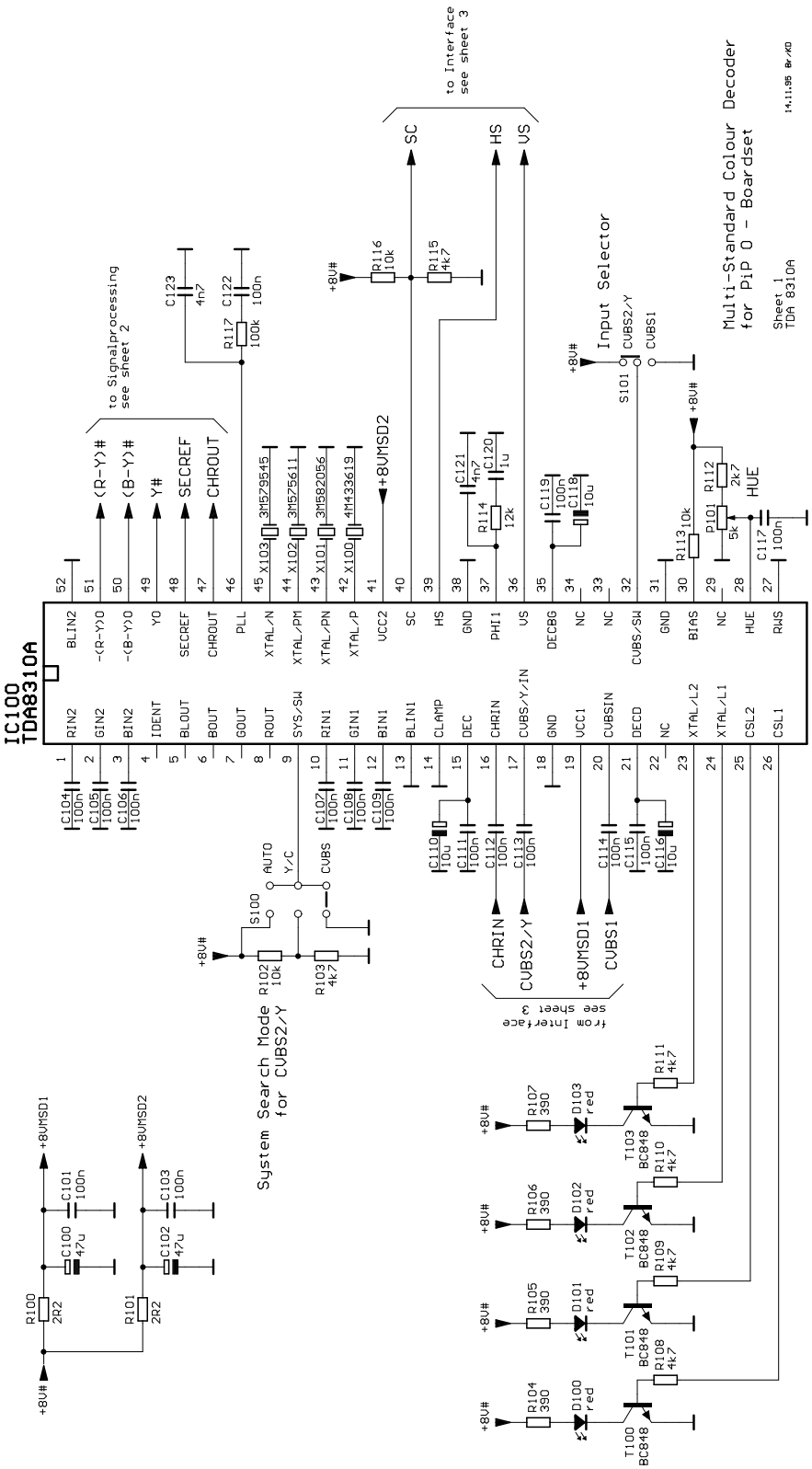


Fig.30 Application and environment of TDA 8310A

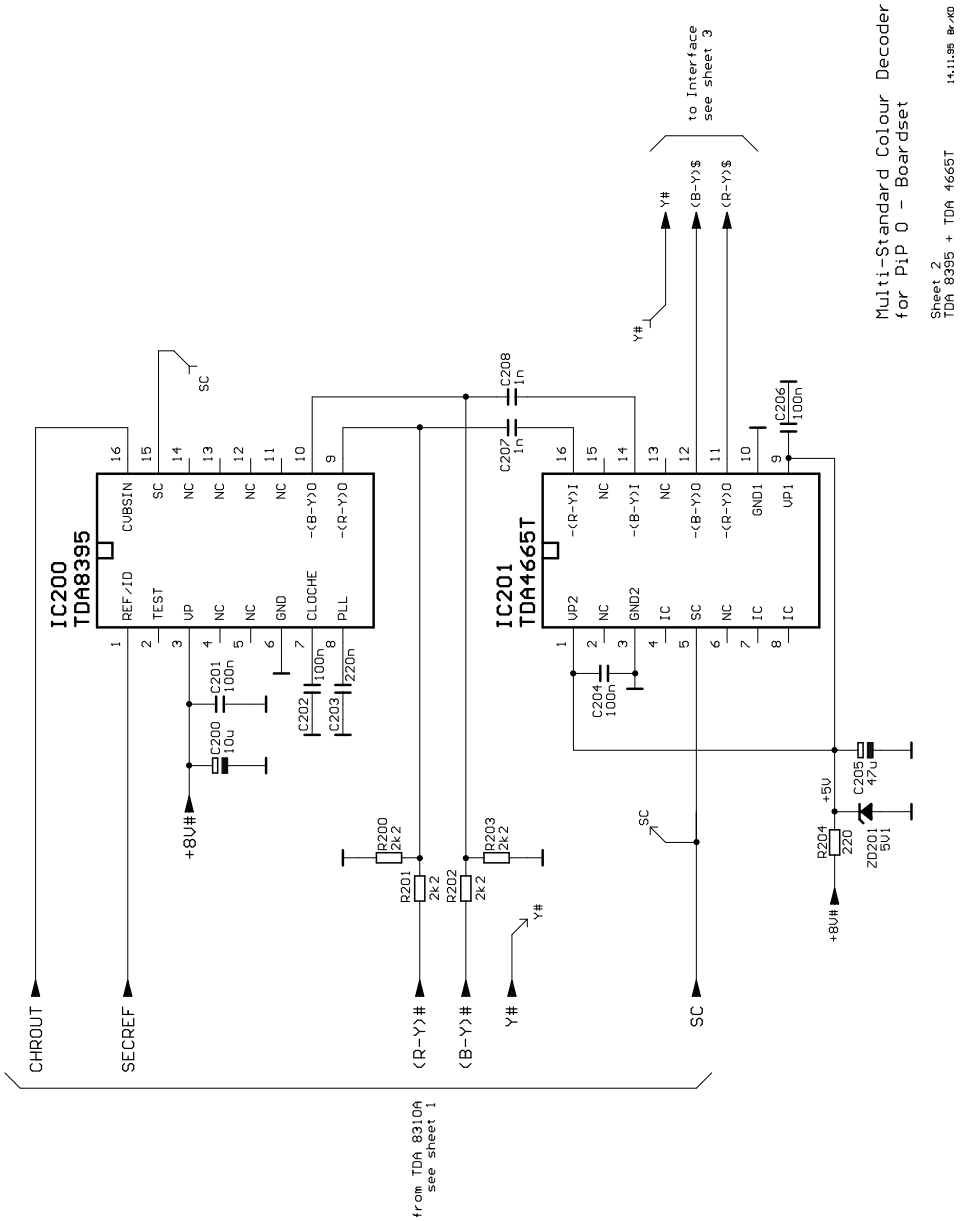


Fig.31 SECAM decoder TDA 8395 and baseband delayline TDA 4665T

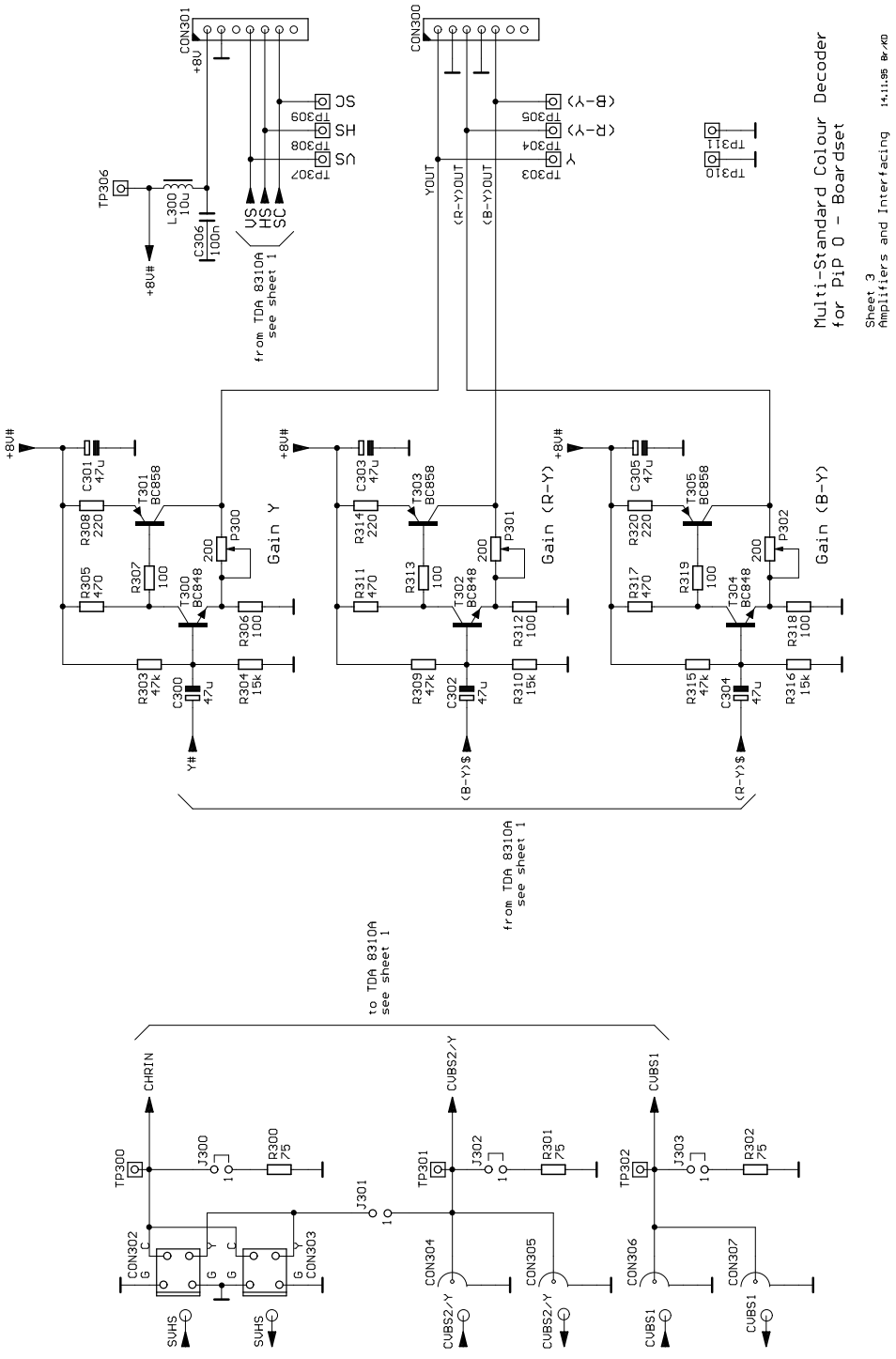


Fig.32 Amplifiers and Interfacing

General

The interface of the multistandard colour decoder module H5VS48 to the PiP controller main PCB is pin compatible to the NTSC colour decoder H4VS65 and all existing versions of the PiP controller main PCB's.

Inputs

The module has three inputs. The CVBS input signals are connected via four SUBCLIC connectors to the PCB and the Y/C input signals are connected via two HOSIDEN SVHS connectors. Each CVBS input and the Y/C input are designed as bridging-type inputs. This allows the module to be connected to a token ring system without using any T-adapters. In case of using this option, the 75 Ω termination has to be disabled.
The 75 Ω termination of the CVBS inputs CVBS1 and CVBS2/Y is enabled if the jumper J303 and J301 are set. The input CVBS2/Y is simultaneous the luminance input for using the module for SVHS input signals. For that reason the resistor R301 is the termination for the Y input of the SVHS connectors, too. The chroma input of the SVHS connectors is terminated via jumper J300 and resistor R300. For using the SVHS connector as signal inputs the jumper J301 has to be set and **no other video signal source has to be connected to the CVBS2/Y input connectors CON304 and CON305**.
The input signals CHRIN, CVBS2/Y and CVBS1 are connected to the multistandard colour decoder IC TDA 8310A via 100 nF coupling capacitors. So no attention has to be paid to the DC level of the incoming video signals. After passing the coupling capacitors, the input signals are clamped by the multistandard colour decoder IC. The unclamped input signals can be probed at the testpins TP300 (CHRIN), TP301 (CVBS2/Y) and TP302 (CVBS1).
If one of the inputs is unused, the belonging termination jumper should be set, to ground the high impedance input pins of the IC TDA 8310A.

Outputs

The module provides the YUV output signals Y_{out}, $(B\text{-}Y)_{out}$ and $(R\text{-}Y)_{out}$ at the belonging pin 1, 3 and 5 of connector CON300. The pins in between the signal pins (pin 2 and 4) lead ground potential for shielding purposes. The output signals are amplified to desired level of the PiP controller inputs. The amplifiers provide the output signals with an output impedance of less than 75 Ω. The output signals can be probed at the testpins TP303 (Y), TP304 (R-Y) and TP305 (B-Y). Ground-testpins are TP310 and TP311.

For synchronization purposes the IC output signals HS, VS and SC are directly connected to the pins 4 (VS), pin 5 (HS) and pin 6 (SC). These signals are unbuffered and have the output impedance of the TDA 8130A - pins. The SC output of the TDA 8310A needs a resistor network to adjust the signal level during H- or V-signal occurrence. The reason for this need is the configuration of the output stage of the IC at pin 40 (SC). The output stage is a simple CMOS driver, made out of one PMOS and one NMOS transistor, see Fig. 33 .

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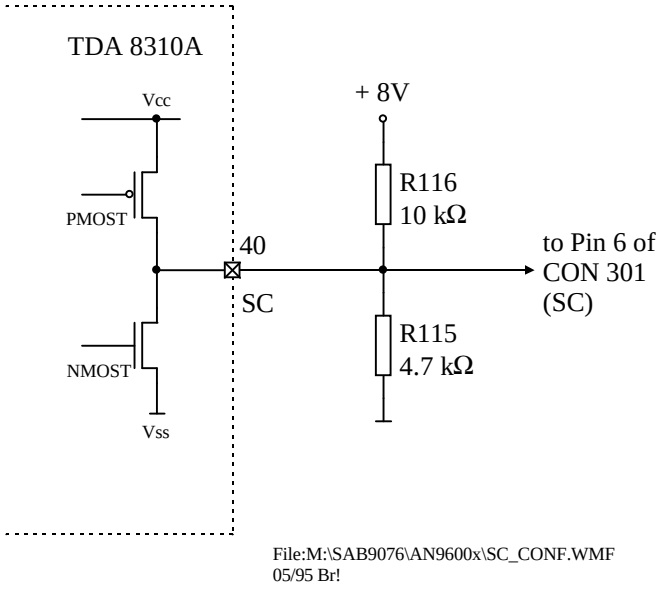

Fig.33 Output configuration of SC pin (TDA 8310A)

The PMOS transistor is switched on during burst key and pulls pin 40 (SC) up to the positive supply. During the active line period (scan mode) the NMOS transistor is switched on and pulls pin 40 down to ground. No one of the transistors is switched on, when a H pulse or a V pulse is active. In fact the output is in threestate. This gives the opportunity to set the SC signal level during H- or V-pulses to a desired value via an external network. In the application of the TDA 8310A, this external network is represented by the resistors R116 and R115.

IC controls

The selection of the two CVBS inputs of the multistandard decoder IC is arranged by the switching voltage applied to pin 32 (CVBS/SW) of the IC. Applying a DC voltage < 1.0 V to this control pin selects CVBS1 for the signal to be demodulated. CVBS2/Y input is selected when the DC voltage at pin 32 exceeds 3.9 V.

If CVBS2/Y input signal is selected the multistandard colour decoder TDA 8310A is able to handle CVBS- and Y/C signals for processing. The mode selection can be done internally by the automatic Y/C detection circuit or can be forced by an external DC control voltage, applied to pin 9 (SYS/SW). This control input is a three level input. If the DC voltage applied to this pin is below 1.0V, the IC is forced into CVBS mode and expects a complete CVBS signal at pin 17 (CVBS2/Y). The chrominance input is disabled in this case.
The external system force into Y/C mode in obtained by applying a DC voltage of between 2.0 V and 3.0 V to pin 9. If the control voltage at pin 9 exceeds 3.9V, the internal automatic Y/C detector arranges the mode control. Depending on the input signal applied to pin 17 (CVBS2/Y) the automatic Y/C detector decides if the IC has to be set into CVBS mode with chroma trap- and chroma band-pass filter active and chroma input disabled or into Y/C mode with bypassed filters and activated chroma input.

The selection between the two CVBS inputs and the possible modes of the IC is designed with two switches S101 and S100. The voltage divider (R 102, R 103) parallel to S100 generates the medium switching voltage for setting pin 9 (SYS/SW) between 2.0 V and 3.0 V.

The adjustment of HUE is obtained a DC voltage, referenced to the control curves shown in Fig. 27 . On the module H5VS48 the control voltage is derived from the 8V supply via a series resistor of 2.7 kΩ and a potentiometer of 5 kΩ to ground. The derived control voltages are lead to pin 28 (HUE) of the IC. This pin is decoupled with a 47nF capacitor to ground to removed any noise on the control voltage and to avoid the modulation of the HUE adjustment by low frequency noise.

Handshake communication between TDA 8310A and TDA 8395

The communication about the identification of SECAM colour coded input signal takes place via the connection between pin SECREF (pin 48) of the TDA 8310A and pin REF/ID (pin 1) of the TDA 8395.
This line carries two informations: a DC voltage, to indicated an identified SECAM input signal and simultaneously added onto the DC voltage, the subcarrier reference signal for the SECAM colour decoder.
Pin 48 (SECREF) of the TDA 8310A provides the subcarrier reference frequency, if the crystal for PAL B/G is used. This is the case when PAL B/G **or no colour standard** is identified. SECAM is for the TDA 8310A **no colour standard** to be identified. For NTSC the subcarrier signal is blanked on pin 48. The DC voltage is 1.6 V for all these cases.
A SECAM coded input signal will not be identified by the TDA 8310A, but the IC provides the subcarrier reference signal of the PAL B/G crystal at pin 48 and the chrominance signal at pin 47. These signals are fed to the SECAM add-on colour decoder TDA 8395 and allow that IC to identify the SECAM signal. When the TDA 8395 identifies the incoming chrominance signal as a SECAM signal, it sinks a current of at least 120µA out of pin 48 of the TDA 8310A. The current indicates the TDA 8310A, that the SECAM decoder has identified the colour standard of the incoming CVBS signal. As a result the TDA 8310A switches his own (R-Y) and (B-Y) outputs in a highohmig threestate, blanks the subcarrier reference signal at pin 48 for the scanning period of a field and sets the DC voltage at pin 48 to at least 4.3 V.
This DC voltage indicates the TDA 8395, that the multistandard colour decoder TDA 8310A is prepared for SECAM. Consequently the TDA 8395 switches his own (R-Y) and (B-Y) outputs into active state.

Loop Filters

For the loop filter of the line oscillator, connected to pin 37 (PHI1), a serial combination of a 12 kΩ resistor and a 1µF capacitor, together with a 4.7nF capacitor in parallel to ground are used.
For the loop filter of the subcarrier oscillator, connected to pin 46 (PLL), we recommend a series combination of a 100 kΩ resistor and a 100 nF capacitor, together with a 4.7nF capacitor in parallel to ground.
This configuration gives the best results in case of phase stability in locked condition and in case of lock-in behaviour.

Crystals

The reference elements for the subcarrier oscillator are crystals, especially performed for colour decoders of the TDA83xx family. **These crystals need no serial load capacitors.**:

TABLE 9 Used Crystals on H5VS48 for TDA 8310A

Condition	Colour Standard	Frequency	12NC - Code
Application without serial load capacitor	PAL / BG	4.433619 MHz	9922 520 00384
	PAL / N	3.582056 MHz	9922 520 00381
	PAL / M	3.575611 MHz	9922 520 00383
	NTSC / M	3.579545 MHz	9922 520 00382

Colour standard indication

For indication the identified colour standard of the incoming CVBS- or Y/C input signal, the control inputs/outputs XTAL/L2, XTAL/L1, CSL2 and CSL1 are used as indent outputs.The outputs CSL1 and CSL2 indicate the identified colour standard and the other two ident outputs indicate the used crystal. All outputs are buffers with a SMD-transistor to drive a LED. The Table 10 shows the activated LED's in respect to the identified colour standard.

TABLE 10 Indication of recognized colour standards

LED indicators	Identified Colour Standard						
	No Colour	PAL B/G	NTSC M	SECAM	NTSC 4.4	PAL N	PAL M
XTAL/L2; Pin 23; D107	-	-	-	-	-	X	X
XTAL/L1; Pin 24; D106	-	-	X	-	-	X	-
CSL2; Pin 25; D105	-	-	X	X	X	-	-
CSL1; Pin 26; D104	-	X	-	X	-	X	X
- ~> LED =off			X~> LED =on				

Decoupling

The IC has it's own bandgap reference, to generate all bias currents and reference voltages, which are internally needed. To protect this major internal node from noise, it has to be decoupled externally by a parallel combination of an electrolytic capacitor of 10µF and a capacitor of 100nF. This combination is connected to pin 35 (DECBG) of the IC and should be grounded to a "quiet" ground potential.

The internal supply rail for the digital part of the IC should be decoupled with an electrolytic capacitor of 10µF and a 100nF capacitor, connected to pin 21 (DECD).

The circuitry for the internal filter tuning needs to be decoupled to obtain the filter adjustment with a good performance. For this, a combination of an electrolytic capacitor of 10µF and a capacitor of 100nF is connected to pin 15 (DEC) of the IC. The capacitor should be connected to a "quiet" ground potential, too.

Supply

The two supply pins 19 (Vcc1) and 41 (Vcc2) of the IC TDA 8310A have a decoupling circuit each. The IC TDA 8395 (SECAM decoder) and the baseband delay line TDA 4665T have their own decoupling circuitry.
A speciality of the baseband delay line TDA 4665T is the supply with + 5V. This supply is generated by a serial resistor of 220 Ω (R204) and a Zener diode (ZD201/5.1V). The output amplifiers are supplied directly from the + 8V and have their decoupling capacitor of 47µF each.
All supplies are derived from the + 8V supply, connected to pin 1 of the connector CON301.
Near to the supply input of the PCB the capacitor C306 and the coil L300 are located, to removed disturbances from the external supply. The supply voltage can be probed at testpin TP306 against one of the ground testpins TP310 or TP311. The proposed supply network and decoupling combinations shown on the schematics are optimized to fulfil two major conditions:

1. The distortions, generated by the IC's itself should be kept as internal as possible and shouldn't be emitted on the supply system and to the opposite supply input of the same IC(e.g TDA 8310A) or to other components placed on the PCB.
2. The distortions in the supply system, especially due to long supply lines, shouldn't reach the supply pins of the IC.

The chosen application is thought to meet the requirements of the PiP Boardset. For applications of the TDA 8310A in other environments, the decoupling combination can be different.

4.2.3 Interface, Probing and Adjustments

The following Fig. 34 shows the placement of all major elements for adjusting or setting the IC as well as the location of the most interesting output signals of the PCB.
Table 11 lists the relevant data of the signals on the interface connectors.

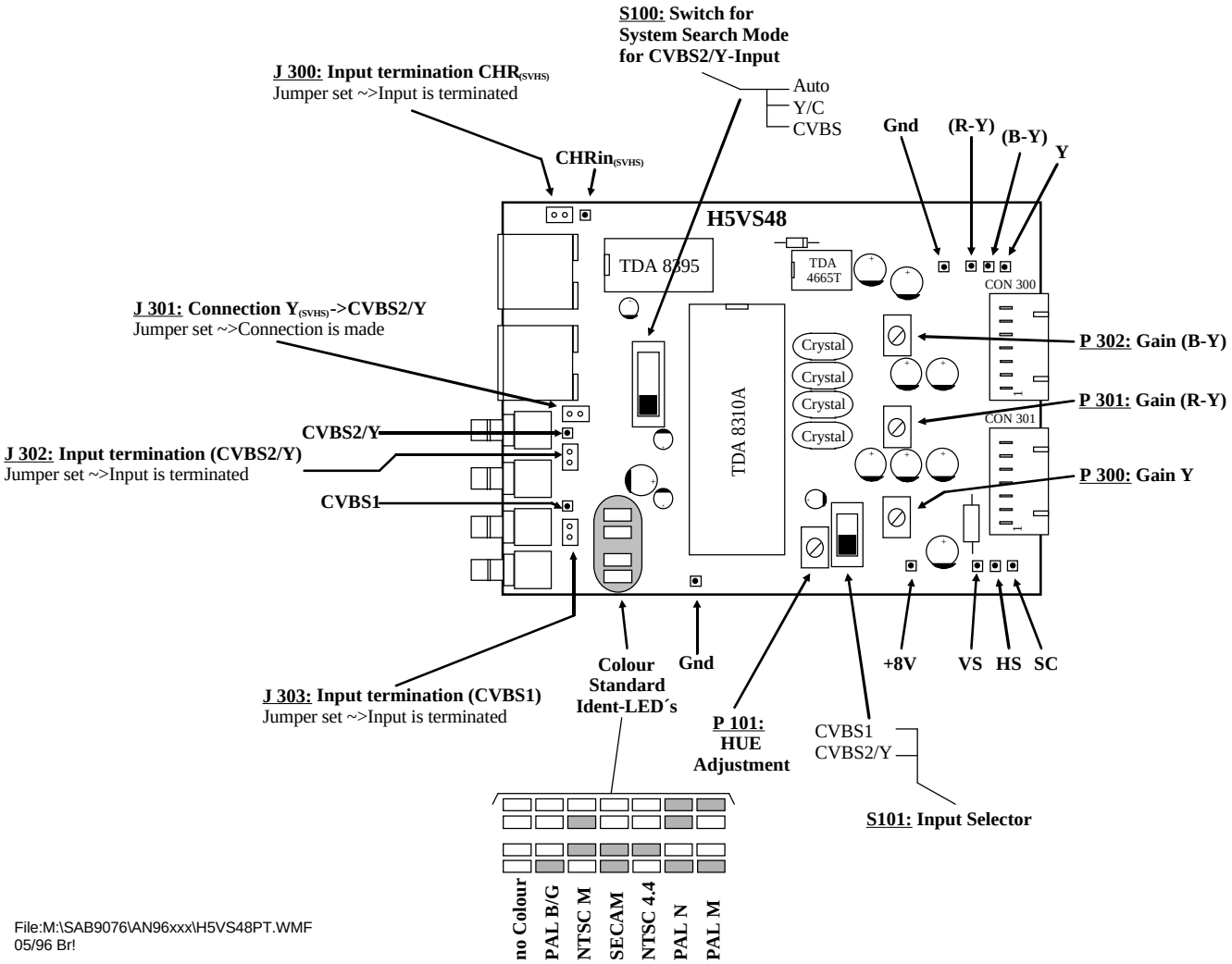

Fig.34 Relevant signals, settings and adjustments of H5VS48

TABLE 11 Characteristics of Interface-signals

Cond.: PAL Standard Colour Bar Testsignal 100/0/75/0; Supply = 8V						
Signal-name	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
CVBS1	1.0 Vpp	-	-	-	-	Video: 700 mVpp Sync : 300 mVpp any DC-Level Input termination: 75 Ω
CVBS2/Y	1.0 Vpp	-	-	-	-	Video: 700 mVpp Sync : 300 mVpp any DC-Level Input termination: 75 Ω
Y_{in}(SVHS)	1.0 Vpp	-	-	-	-	Video: 700 mVpp Sync : 300 mVpp any DC-Level Input termination: 75 Ω
CHR_{in} (SVHS)	650 mVpp	-	-	-	-	Chroma: 650 mVpp any DC-Level Input termination: 75 Ω
Y	2.0 Vpp	0.4 V Sync Bottom	2.4 V White peak	-	64 µs	Black-Level = 0.9V_{DC} Luminance = 1.5 Vpp
-(B-Y)	1.5 Vpp	0.5 V	2.0 V	-	64 µs	no-colour-Level = 1.25V_{DC}
-(R-Y)	1.5 Vpp	0.75 V	2.25 V		64 µs	no-colour-Level = 1.5V_{DC}
H	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	-
V	5.2 Vpp	0 V	5.2V	320 µs	20 ms	-
SC	4.8 Vpp	0 V	4.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 910µs	64 µs	Burst-Key-Top =4.8 V_{DC} H-Pulse-Top = 2.4 V_{DC} V-Pulse-Top = 2.4 V_{DC}
+8V	-	-	-	-	-	Supply Voltage

4.2.4 Layout and Placement

The following figures show the layout and placement for the H5VS48 module in original size.

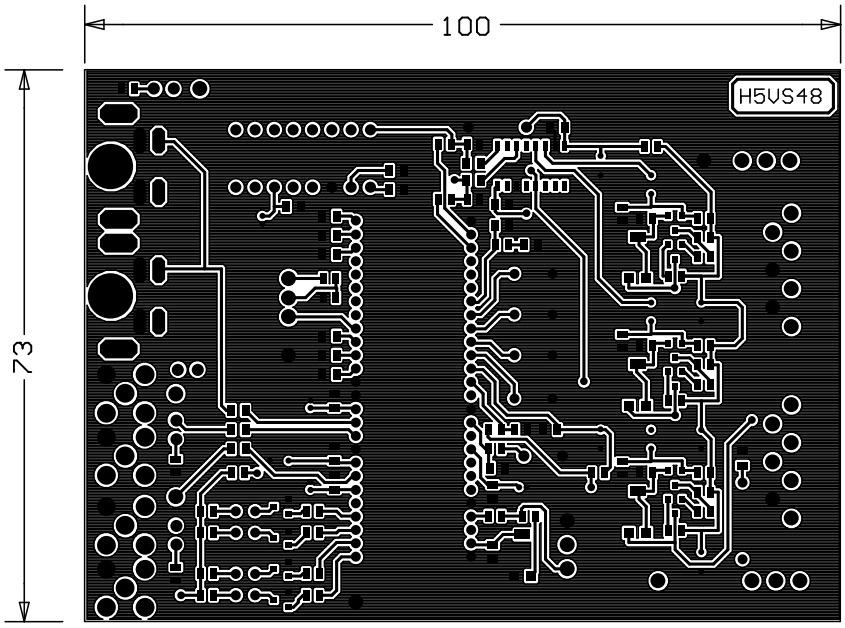

Fig.35 Layout of H5VS48 Topside

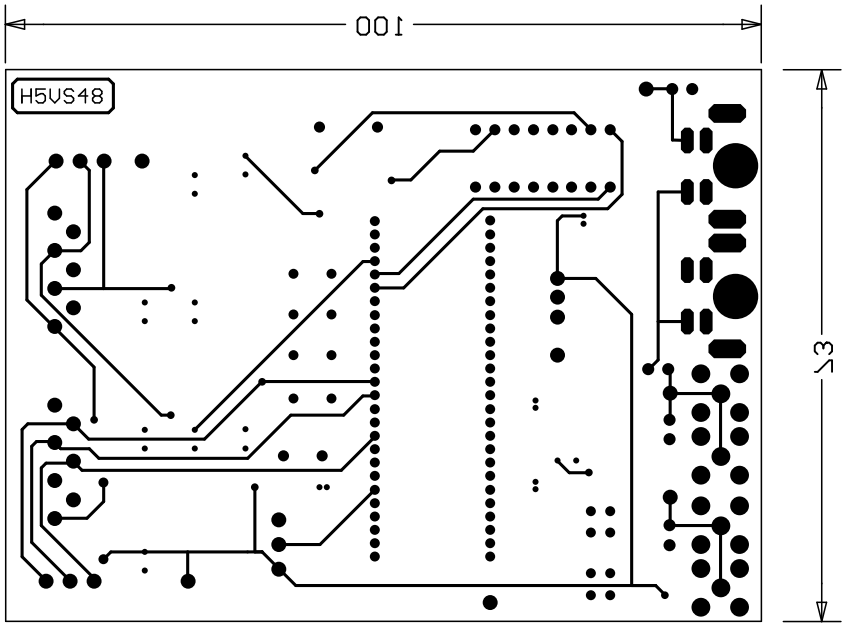

Fig.36 Layout of H5VS48 Bottomside

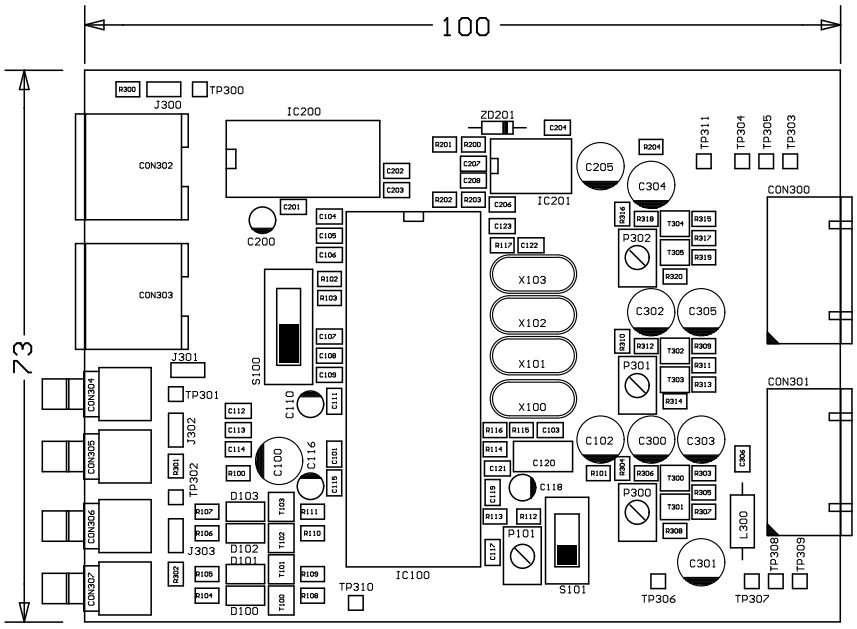

Fig.37 Placement of Topside - Components

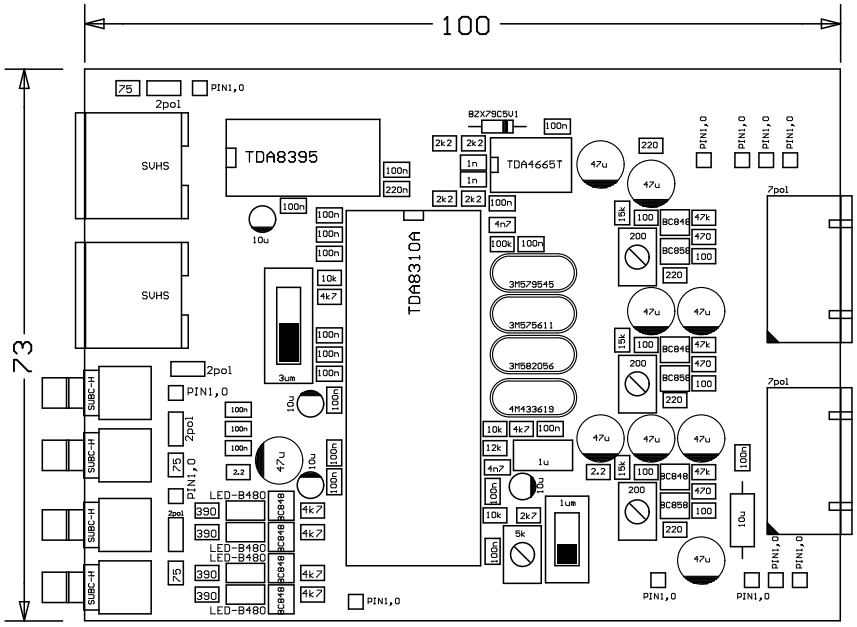

Fig.38 Values of Topside - Components

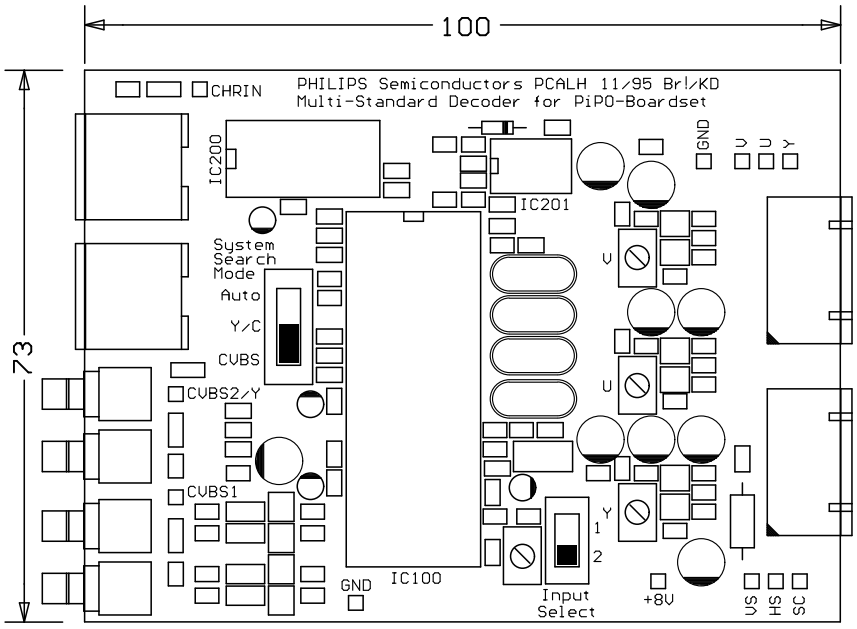

Fig.39 Topside - Printing

4.2.5 Application hints

The multistandard colour decoder module H5VS48 is designed as a double sided PCB. The components are placed on the topside only for simplifying probing, testing and evaluation. For implementation the circuitry in an environmental PCB design the components can be placed on the bottomside and a multilayer design is possible even, too.

It should be taken care of the distance between the decoupling elements and the IC's as well as between the TDA 8310A and the SECAM add-on decoder TDA 8395. The lines for conducting the SECAM reference signal and the chrominance signal to the TDA 8395 should be designed as short as possible for preventing them for external disturbances.

4.3 Videoprocessor TDA 4780 on H5VS66

The videoprocessor module H4VS66 contains the high performance video backend IC TDA 4780 for converting the output signals of the PiP controller into the RGB format and to influence the signal parameters like brightness, contrast or saturation.

4.3.1 Description of TDA 4780

Detailed date about this IC you will find in the Philips Semiconductors Databook IC02b [1] and in the application note AN94073 [3].

General description

The TDA 4780 video processor handles two RGB inputs and a YUV input. The signal parameters like brightness, contrast, saturation and gamma are processed internally. The finished signal will be converted to RGB domain and buffered. The IC is fully controllable via I^2C bus. Additional to the videosignal processing the IC includes feedback loops for stabilizing the cut-off current and the peak beam current of the picture tube. These parts of the IC will be not explained here, because they are not used for the PiP application.
A rough blockdiagram is shown in Fig. 40 .

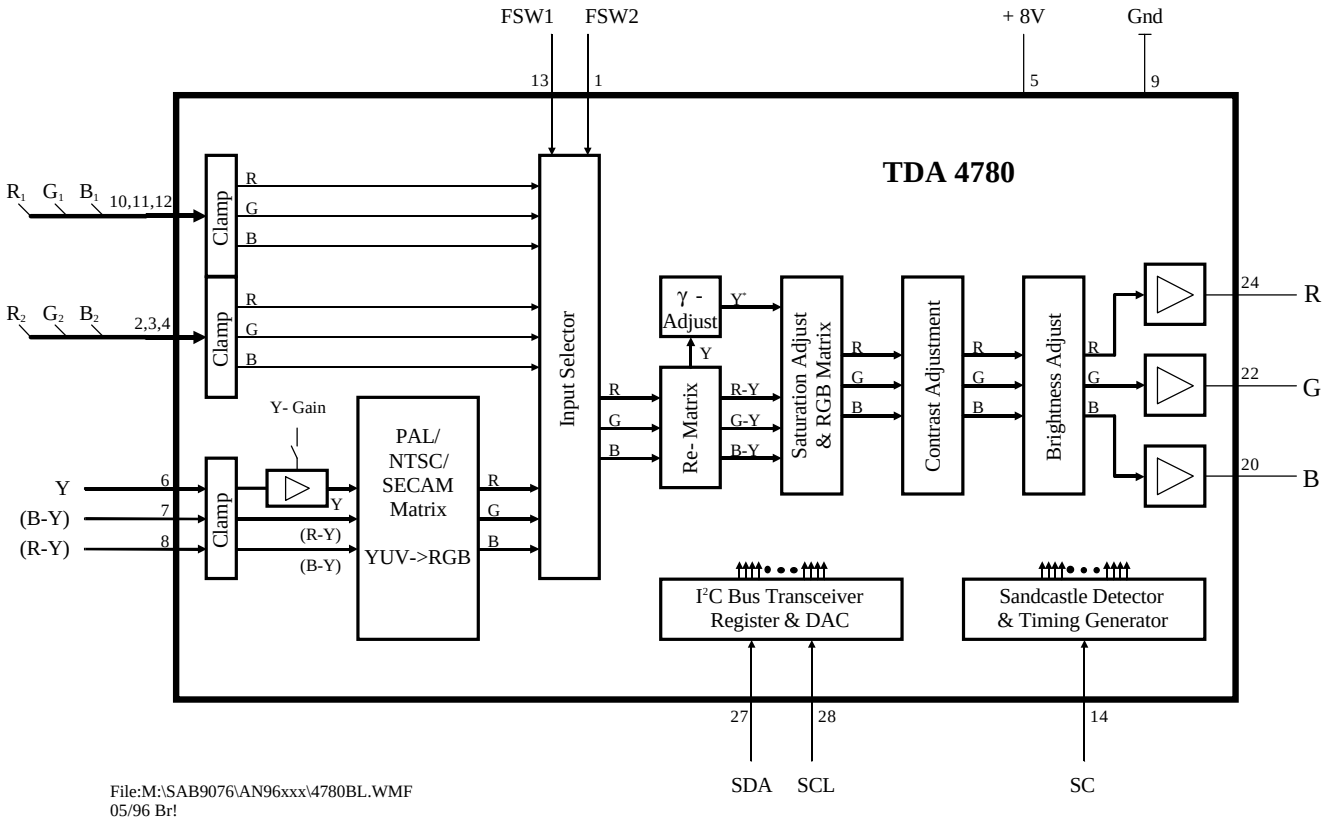

Fig.40 Blockdiagram of Videoprocessor TDA 4780

The signal path which is used for the PiP application is marked with bold lines.

General description

The TDA 4780 is a video signal backend processor IC, which combines two RGB signals and one YUV signal to one RGB output signal. The IC allows to vary the signal parameters of the combined RGB signal like saturation, contrast and brightness. CRT dependent signal parameters like peak white beam current or black level current are controlled and can be influenced, too. Because this part of the IC is not used in the PiP application, it will not be described here.
All settings of the IC can be made by I^2C bus.

Video processing path

The TDA 4780 has two RGB inputs with their associated fast switch inputs. The RGB input signals are clamped to an internal reference voltage and fed to an input selector matrix.
The YUV input signals are clamped to an internal reference voltage, too. The luminance signal passes an amplifier with two switchable gain factors for adapting the TDA 4780 to several video processing IC's in front of the TDA 4780. The corrected and clamped luminance and colour difference input signals are converted into the RGB domain by the NTSC/PAL-SECAM matrix. The different matrix coefficients for either PAL-SECAM or NTSC are selected by an I^2C bus register.
The input selector matrix is controlled by the input voltages FSW_1 and FSW_2. The first multiplexer, controlled by FSW_1, selects between the YUV input signals and the $(RGB)_1$ input signals. The selected output signal is fed to the second multiplexer, controlled by FSW_2 for combining it with the $(RGB)_2$ input signals.

TABLE 12 Input signal selection

FSW_2	FSW_1	$(RGB)_2$ inputs	$(RGB)_1$ inputs	YUV inputs	Output signals
0	0			→	→
0	1		→	→	→
1	0	→	→	→	→
1	1	→	→	→	→

The output signals from the input selector matrix is fed to a re-matrix, which re-builds the luminance component out of the incoming RGB signals and subtracts it from the RGB signals.
The luminance signal is nonlinear amplified by the γ-correction stage, which is active in the low level region only. The luminance reduced RGB signals (R-Y), (G-Y) and (B-Y) are amplified in order to get a saturation control. The saturation control block contains a matrix to combine the saturation adjusted (RGB)-Y signals together with γ-corrected luminance signal to a complete RGB signal. The output signal of this block is fed to the contrast adjustment stage and then to the brightness adjustment stage. The last stages in the video processing signal path are three output buffers with an output impedance of less than 30Ω each.

Timing and controlling

The IC needs a lot of periodical timing- and control signals. All timing- and control signals are derived from a sandcastle pulse, connected to pin 14 of the IC. The internal servo loops, which incorporate the behaviour of the CRT need this timing- and control pulses too. For offering the most flexibility to the user, the input of the sandcastle detector is adaptable to the two existing layouts of the sandcastle pulse.
The sandcastle detector is able to work with the conventional 12V/8V-sandcastle and with the modern 5V sandcastle. The different signal forms and signal thresholds are shown in Fig. 41 .

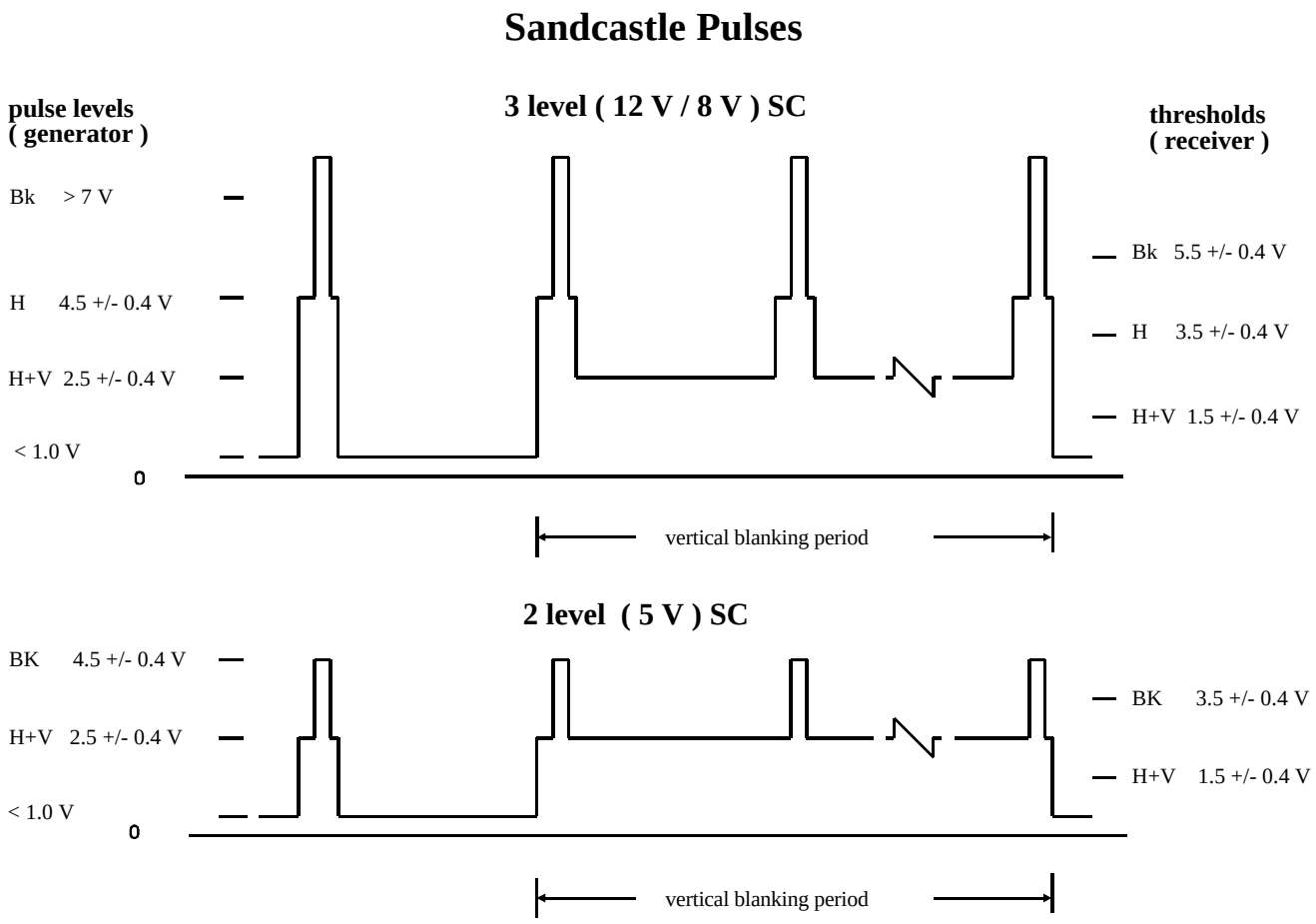

Fig.41 Signal forms and thresholds of two- and three level sandcastle pulses

The selection between the two types of the sandcastle pulse is made by the I^2C bus and a associated register bit.

4.3.2 Description of I^2C-Bus registers and default values

Description of I^2C-Bus registers

All major functions of the IC and the video signal parameter variations are controlled and/or adjusted by I^2C bus. The device address of the IC is 88_{Hex}. This address is fix. The IC is not prepared to read out the data of the internal I^2C bus registers.
The IC has 15 internal I^2C-bus register, where 12 registers contain numerical values to adjust the video signal parameters and where three registers contain 8 bit words for controlling the IC. Every bit of these words has a control function.
This chapter describes the meaning of the I^2C bus register bits in a very rough form. For more detailed information please look for the application note AN94072 [3] and for the booklet [4].

TABLE 13 I^2C bus register of TDA 4780

Function	Sub-address	Data Bytes							
		D7	D6	D5	D4	D3	D2	D1	D0
Brightness	00_{Hex}	0	0	A05	A04	A03	A02	A01	A00
Saturation	01_{Hex}	0	0	A15	A14	A13	A12	A11	A10
Contrast	02_{Hex}	0	0	A25	A24	A23	A22	A21	A20
Hue	03_{Hex}	0	0	A35	A34	A33	A32	A31	A30
Red gain	04_{Hex}	0	0	A45	A44	A43	A42	A41	A40
Green gain	05_{Hex}	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06_{Hex}	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07_{Hex}	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08_{Hex}	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09_{Hex}	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	$0A_{Hex}$	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Gamma	$0B_{Hex}$	0	0	AB5	AB4	AB3	AB2	AB1	AB0
Control register 1	$0C_{Hex}$	SC5	DELOF	BREN	X	NMEN	X	X	X
Control register 2	$0D_{Hex}$	X	HDTV	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Control register 3	$0E_{Hex}$	ADBL	YHI	MOD2	BLST	YEXH	RELC	TCPL	0

I^2C bus register for video signal adjusting

The register 00_{Hex} to $0B_{Hex}$ contain 6 bit words, so the corresponding parameter can be varied in 64 steps. The 6 bit words are converted internally to an analog control voltage.
The default value for the first three register (Brightness, Saturation and Contrast) can be set to 20_{Hex} and therefore to the middle of the allowed value range. Increasing the register values increases the video signal parameters. Decreasing the register values decreases the video signal parameters down to zero (no brightness, no colour, no contrast).For compensating some tolerances, in case of a power reset the default values are set to 28_{Hex} for brightness, 20_{Hex} for saturation and 22_{Hex} for contrast.

The HUE register content is converted to an analog control voltage, which is available at pin 26 of the IC (YHUE). The control voltage at pin 26 is intended for colour decoder IC's, which need a HUE control voltage for demodulating NTSC video signals. The default value of the register 03_{Hex} is 20_{Hex}. So the variation range for positive HUE shift is the same as for the negative HUE shift.

The values in the register 04_{Hex}, 05_{Hex}, 06_{Hex} adjust the gain of the RGB output amplifiers. These controls are intended for adjusting the white balance of the TV set.The default values of the register are 20_{Hex} for each register.

The register 07_{Hex}, 08_{Hex}, and 09_{Hex} contain reference values for the cut-off automatic function of the IC. This function works only together with an attached picture tube. The default values of the register are 20_{Hex} for each register.

Register $0A_{Hex}$ contains a reference value for the peak drive limiter. The circuitry limits the maximal beam current of the picture tube and needs for correct operation a feedback voltage from the CRT. Without this feedback voltage the circuitry limits the amplitude of the RGB output signals independent of the CRT. The default value for this register is $3F_{Hex}$.

The register $0B_{Hex}$ contains the value for the γ-correction. The γ-correction is a non-linear amplification of low-level luminance signals. A strong γ-correction makes more details visible in dark pictures, but it gains the noise, too. The default value in this register is 00_{Hex} for no γ-correction (linear luminance signal processing).

Control register

The control register have to be explained bit by bit.

Control register 1

TABLE 14 Control register 1 of TDA 4780

Function	Sub-address	Data Bytes							
		D7	D6	D5	D4	D3	D2	D1	D0
Control register 1	$0C_{Hex}$	SC5	DELOF	BREN	X	NMEN	X	X	X

- SC5

  Sand**C**astle **5**V: selects the comparator voltage levels in the sandcastle pulse detector
  0--> comparator levels for a three-level, > 8V sandcastle pulse selected
  1--> comparator levels for a two-level, 5V sandcastle pulse selected.

- DELOF

  DELay **OF**f: enables/disables a delay of approximately 5µs in the leading edge of the black level clamping pulses
  0--> clamping pulse delay enabled
  1--> clamping pulse delay disabled.

- BREN

  Buffer **R**egister **EN**able: selects buffer register storage in the IIC-bus receiver during data transfer
  0--> new data immediately executed, auto-increment possible
  1--> received data is first stored in a buffer register in the IIC-bus transceiver and is fed to the data registers in the next vertical blanking interval.

- NMEN

  NTSC **M**atrix **EN**able: enables/disables the NTSC matrix
  0--> PAL/SECAM matrix selected
  1--> NTSC matrix selected.

Control register 2

TABLE 15 Control register 2 of TDA 4780

Function	Sub-address	Data Bytes							
		D7	D6	D5	D4	D3	D2	D1	D0
Control register 2	$0D_{Hex}$	X	HDTV	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1

- HDTV

  High **D**efinition **TV**: selects the active line numbers for standard TV- or HDTV / Progressive Scan mode of the (ADBL) adaptive black level control line counter.
  0--> 272 lines at PAL/SECAM, 224 lines at NTSC
  1--> 544 lines at PAL/SECAM, 448 lines at NTSC

- FSBL

  Full **S**creen **B**lack **L**evel: selects the duration of the artificial black level
  0--> the artificial black level is selected only during the measurement pulses for cut-off control (nominal)
  the artificial black level is continuously selected for all three colour channels;
  the artificial black level is continuously displayed during vertical scan
  for optical measurements (automatic cut-off control operates normally).

- BCOF

  Black Level **C**ontrol **OF**f: enables/disables automatic cut-off control
  0--> enables automatic cut-off control
  1--> disables automatic cut-off control, in this case, the RGB outputs are clamped to cut-off levels of 2.5V.

- FSDIS2

  Fast **S**witch **DIS**able **2**: enables/disables FSW2 selection of R2 G2 B2 or the signals selected by FSW1.

- FSON2

  Fast **S**witch **ON 2**: IIC-bus selection of either colour signals R2 G2 B2 or the signals selected by FSW1.

- FSDIS1

  Fast **S**witch **DIS**able **1**: enables/disables FSW1 selection of colour signal R1 G1 B1 or YUV signal.

- FSON1

  Fast **S**witch **ON 1**: IIC-bus selection of either colour signals R1 G1 B1or YUV signals via fast switch 1 (FSW1).

Signal input selection by the IIC-bus control bits, FSW1 and FSW2 is shown in Table 16 .

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TABLE 16 Signal input selection by the fast switches and the I^2C bus register bits

I^2C-bus control bits				analog switch		selected signal and function			
FSON2	FSDIS2	FSON1	FSDIS1	FSW2 pin 1	FSW1 pin 13	RGB1 pin 2 - 4	RGB2 pin 10-12	YUV pin 6 - 8	ADBL *)
L	L	L	L	L	L			ON	ACTIVE
				L	H		ON		ACTIVE
				H	X	ON			OFF
L	L	L	H	L	X			ON	ACTIVE
				H	X	ON			OFF
L	L	H	X	L	X		ON		ACTIVE
				H	X	ON			OFF
L	H	L	L	X	L			ON	ACTIVE
				X	H		ON		ACTIVE
L	H	L	H	X	X			ON	ACTIVE
L	H	H	X	X	X		ON		ACTIVE
H	L	X	X	L	X	ON			ACTIVE
				H	X	ON			OFF
H	H	X	X	X	X	ON			ACTIVE

Remarks on the table:

*) ADBL ACTIVE means the function is set by the ADBL bit;
OFF means the function is internally switched off independent on setting of the bit ADBL.

H is a logic HIGH or analog switch (pins 1 and 13) to > 0.9V
L is a logic LOW or analog switch (pins 1 and 13) to < 0.4V,
(these logic levels also apply to FSW1 and FSW2),
X is “don’t care”
ON is the selected signal input.

Control register R3

TABLE 17 Control register 3 of TDA 4780

Function	Sub-address	Data Bytes							
		D7	D6	D5	D4	D3	D2	D1	D0
Control register 3	$0E_{Hex}$	ADBL	YHI	MOD2	BLST	YEXH	RELC	TCPL	0

- ADBL

ADaptive **BL**ack: enables/disables adaptive black control
0--> adaptive black control disabled
1--> adaptive black control enabled

- YHI

  YHigh **I**nput level: selected the nominal input level of Y-signal input pin 8.
  0--> nominal input level is 0.315 V (VB) (black-white)
  1--> nominal input level is 1.0 V (VB) (black-white)

- MOD2

  MODus **2**: disables/enables the internal brightness control stage. This mode should only be used in case of RGB output clamping. Thus, precondition for MOD 2 is back level control off, bit BCOF = 1.
  The application is:
  1. CRT signal drive without cut-off control or LCD signal drive, bit setting MOD 2 = 0, BCOF = 1;
  2. provide RGB output signals for a RGB interface or LCD signal drive both without brightness control, bit setting MOD 2 = 1, BCOF = 1;
  0--> Brightness control enabled
  1--> Brightness control disabled

- BLST

  BLue **ST**retch: enables/disables the blue stretch function.
  0--> Blue stretch off
  1--> Blue stretch on

- YEXH

  Y EXclusive **H**ue: switches either a Y signal for the scan velocity modulation (SCAVEM) application or the Hue control voltage for a multi standard decoder to the pin 26.
  0--> The hue adjust output is switched to pin 26
  1--> The Y output for SCAVEM is switched to pin 26

- RELC

  RELative to **C**ut-off: selects the peak drive limiter mode. The chosen peak drive limit can be either to the absolute output level (old PDL) or to the relative output level referred to the cut-off level (new PDL).
  0--> Peak drive limit to absolute output level
  1--> Peak drive limit relative to cut-off level

- TCPL

  Time **C**onstant **P**eak drive **L**imiter:
  selects the time constant of peak drive limiter either for single- or double line frequency application (100Hz or progressive scan).
  0--> time constant for 2 fH
  1--> time constant for 1 fH

Default values for the I^2C bus register

Table 18 lists the default values for the 15 I^2C bus register for the TDA 4780 in the PiP application.

TABLE 18 Default settings of TDA 4780 for PiP application

Register Subaddress	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Default Data	28	20	22	20	20	20	20	20	20	20	3F	00	C1	1A	00

4.3.3 Description of the video processor module H4VS66

The video processor module H4VS66 is the interface between the PiP controller and the SCART input of a monitor or TV set. The module provides RGB inputs as well as the YUV inputs from the PiP controller. For synchronization a sandcastle pulse has to be delivered. This pulse may come from either an external colour decoder or from the main channel colour decoder of the PiP concept.
The blockdiagram of the video processor module H4VS66 is shown in Fig. 42 .

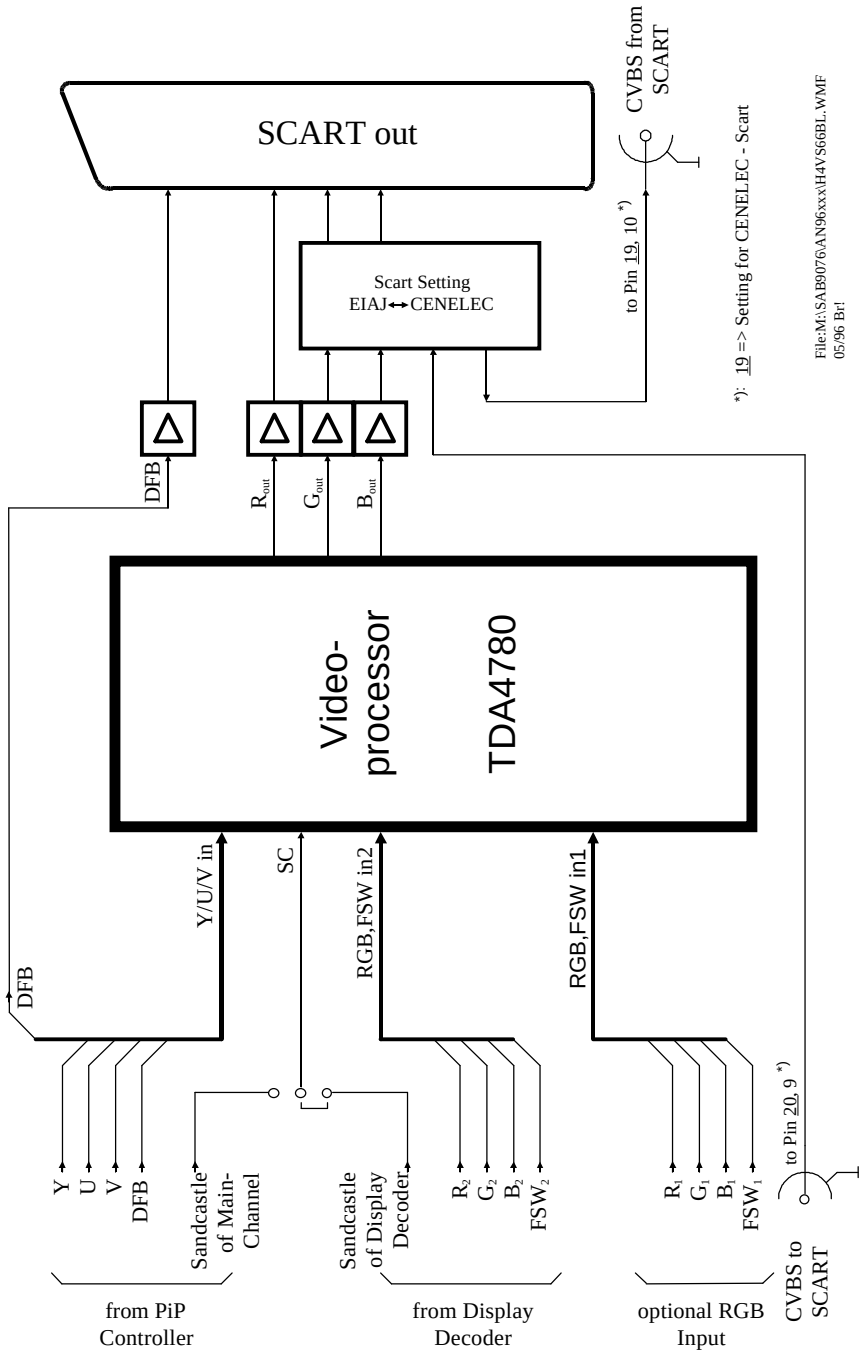


Fig.42 Blockdiagram of video processor module H4VS66

Fig. 43 shows the schematics of the module H4VS66.

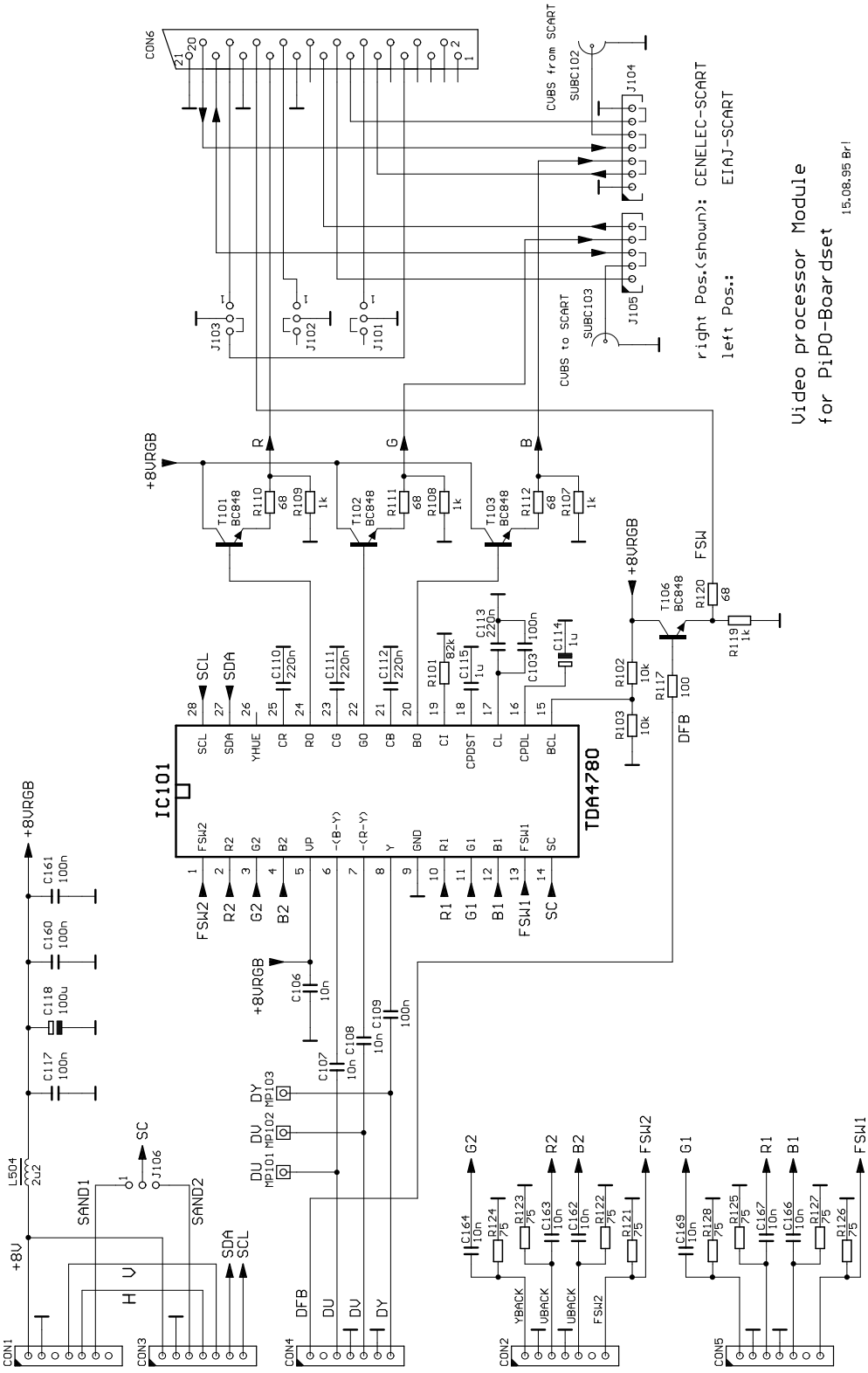


Fig.43 Schematics of video processor module H4VS66

General

The video processor module H4VS66 is the interface between the PiP controller main PCB and a SCART input of a monitor or a TV set. The module provides the feature to insert the output signals from the PiP controller into several RGB signals. Additional the YUV output signals of the PiP controller are converted into the RGB domain. Input signals for the background can be taken either from the RGB inputs of the module or from the SCART plug.

Inputs

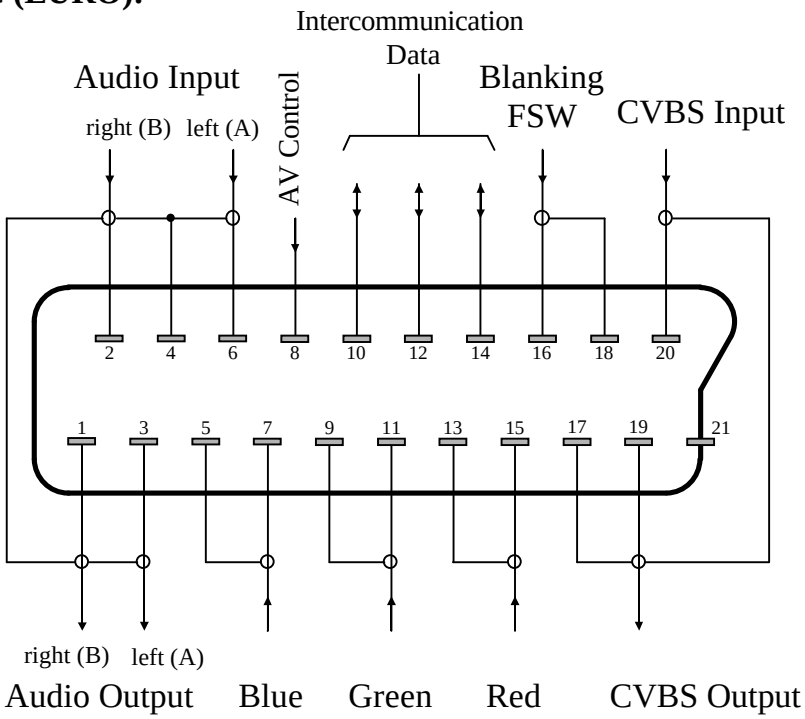
The main inputs are the YUV signals coming from the PiP controller. These signals together with an associated fast blank pulse are provided to connector CON4 of the PCB. The YUV signals are AC coupled with 10nF capacitors each to the pin 6,7and 8 of the TDA 4780. Before the coupling/clamping capacitors the input signals can be probed at the testpins MP101 [-(B-Y)], MP 102 [-(R-Y)] and MP 103 [Y]. These input signals are not terminated. The YUV input signals are converted internally to the RGB domain and may be mixed with other external RGB signals.
The input signal DFB, available on pin 1 of connector CON4, is buffered on the PCB and fed directly to pin 16 of the SCART socket CON6. The DFB signal is active, when the processed video signals of the PiP controller are valid.

The module is prepared for processing two independent sets of RGB input signals with their associated fast switch signals.
The first set of RGB input signals can be supplied via connector CON5. The RGB signals are AC coupled with 10nF capacitors each to the pins 10 (R1), 11 (G1) and 12 (B1) of the video processor TDA 4780. Pin 7 of the connector CON5 leads the associated fast switch signal to pin13 of the TDA 4780. All inputs are terminated with 75Ω resistors. The connector CON5 is intended for supplying an external signal from a RGB source like a video signal generator to the PiPO boardset.
The second set of RGB input signals can be supplied via connector CON2. The RGB signals are AC coupled with 10nF each to the pins 2 (R2), 3 (G2) and 4 (B2) of the video processor TDA 4780. Pin 7 of the connector CON2 leads the associated fast switch signal to pin 1 of the TDA 4780. All inputs are terminated with 75Ω resistors. The connector CON2 is intended for supplying RGB signals from the third colour decoder of the PiP boardset as background picture (see concepts on Fig. 16 and Fig. 17).
As a major condition, both sets of RGB signals have to be synchronized to the YUV signals coming from the PiP controller.
Following the idea of modularity and compatibility the connectors CON2 and CON1 are pin compatible to the pinning of the NTSC colour decoder module H4VS65 and the multistandard colour decoder module H5VS48. Therefore the pins 1, 3 and 5 of connector CON2 are video signals inputs. The video processor module H4VS66 expects RGB signals at these inputs, but the colour decoder modules deliver YUV signals. This gives no conflict because pin 7 of CON2 (FSW2) is not applied.
Pin 2 and 4 of connector CON2 lead ground potential for shielding purposes.
Because of the pin compatibility, the synchronisation signals of the third colour decoder are available at pin 4 (V), pin 5 (H) and pin 6 (SC) of connector CON1. The H- and V-signals are necessary for synchronizing the display part of the PiP controller. They are bridged to conncector CON3 to be applied to the PiP main module. The sandcastle signal (SC) is needed to synchronize the video processor TDA 4780.

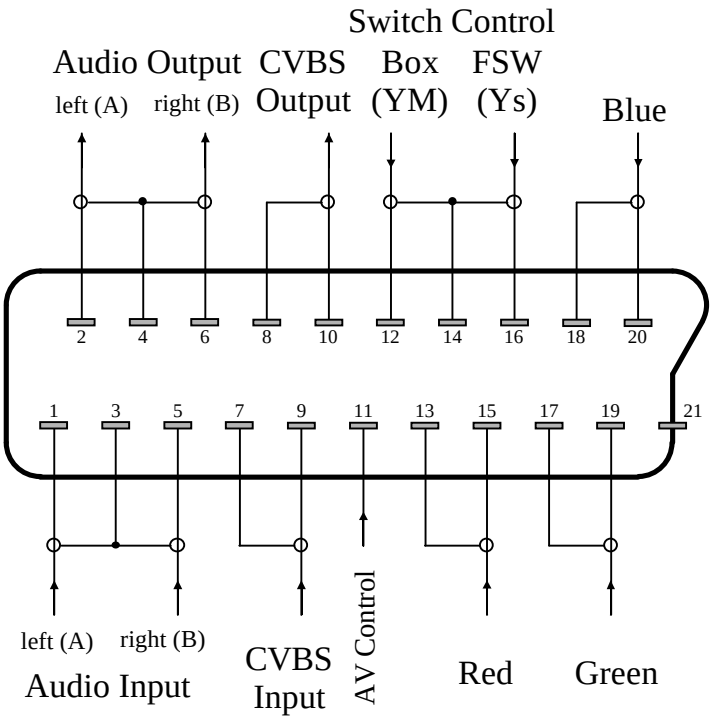
Outputs

The video signals are processed by the TDA 4780 and buffered by 75Ω impedance converters. The R output signal is directly fed to the SCART connector CON6, the G- and B output signals are connected via the jumper banks J102 and J103 to the SCART connector CON6.
The jumper banks J102 and J103 are thought to make the video processor module H4VS66 compatible to the pinning of the european CENELEC-SCART standard and to the pinning of the Japanese EIAJ-SCART standard.Fig. 44 shows the different pinning of the European CENELEC-SCART and the Japanese EIAJ-SCART and Table 19 lists the pins/signals which have to be switched by the jumper banks.

CENELEC (EURO):



EIAJ:



File:M:\SAB9076\AN96xxx\SCART.WMF
06/96 Br!

Fig.44 Pinning of SCART connectors

TABLE 19 Pins and signals to be switched

Pin No.:	CENELEC (EURO)	EIAJ
5	Gnd	open
7	Blue	Gnd
8	open	Gnd
9	Gnd	CVBS input
10	open	CVBS output
11	Green	open
14	open	Gnd
18	open	Gnd
19	CVBS output	Green
20	CVBS input	Blue

The desired pin configuration of the SCART socket is selected by setting the jumper J101, J102, J103 and the jumper banks J104 and J105. The jumpers are located near the SCART socket. The setting of the jumpers are marked with the letters “C” for CENELEC and “E” for EIAJ. Setting all jumpers into the right hand position selects the CENELEC (EURO) pinning standard. Setting all jumpers into the left hand position selects the EIAJ pinning standard.

If the SCART cable is connected to the VCR-SCART socket of a TV set, at pin 20 of the EURO SCART connector CON6 the CVBS signal of the TV set is available. This signal is fed via the jumper bank J104 to the SUBCLIC connector SUBC102. The CVBS signal can be processed further for synchronisation the third colour decoder for example.
On the other hand an external CVBS signal can be fed to the TV set via the SUBCLIC connector SUBC103, the jumper bank J105, pin 19 of the EURO SCART connector and the SCART cable.

IC controls

The video processor TDA 4780 is fully controllable by I^2C bus commands. The two bus lines SDA and SCL are provided at the pins 6 (SDA) and 7 (SCL) of connector CON3, coming from the PiP main module. The signals SDA and SCL can be probed on the PCB at vias, which are named “SDA” and “SCL” (see Fig. 45 under 4.3.4 Interface and Probing).

For synchronizing the video processor TDA 4780, a sandcastle signal is needed. The sandcastle signal can be delivered from the third colour decoder via pin 6 of conncector CON1 or from the main channel colour decoder of the PiP system via pin 3 of conncector CON3. The selection between them is done by the setting of the jumper J106. Setting the jumper J106 into the upper position selects the sandcastle signal from the third colour decoder.

Further application hints for TDA 4780

The special features of the video backend processor TDA 4780 like cut-off current stabilization or peak beam current limiting are designed for an optimal cooperation between the backend processor and the picture tube. Together with a CRT these functions act as servo loops with preseted values by I^2C bus. As in our case, where no CRT is available, the picture tube can be simulated by a simple resistor. This keep the special function alive, but they can’t react as a servo loop anymore.
The simulation of the CRT is done by feeding +4 V into pin 15 (BCL) of the TDA 4780 and connecting pin 19 (CI) via a resistor to ground. The +4 V for pin 15 are derived from the +8 V supply by a simple voltage divider out of

R102 and R103. We recommend a value of 10kΩ for each resistor. The connection of pin 19 to ground is done by R101. We recommend a resistor value of 82kΩ.
To obtain the special function of the TDA 4780, some storage capacitors for keeping analog control voltages are needed.
For storing the control voltage for the cut-off control function a capacitor of 220nF is necessary for each of the three output buffer. These capacitors are connected to the pins 21 (CB), 23 (CG) and 25 (CR) and should be placed as near as possible to the IC pins. Ceramic SMD chip capacitors may be used.
The leakage current compensation needs a capacitor of 330nF at pin 17 (CL) of the TDA 4780 for correct operation. This capacitor should be located as near as possible to the pin, too. A ceramic SMD chip capacitor may be used.
The storage element for the adaptive black level correction circuitry is a capacitor of 1µF, connected to pin 18 (CPDST) of the TDA 4780. Because of the leakage current sensitivity of this circuitry, no electrolytic capacitor can be used for this function. We recommend the use of a ceramic multilayer capacitor, which should be placed as near as possible to the pin of the TDA 4780.
The peak beam limiter needs a capacitor of 1µF to ground as storage element. The capacitor is connected to pin 16 (CPDL) of the TDA 4780. The internal circuitry is not leakage current sensitive as pin 18. For that reason, a normal electrolytic capacitor may be used. The capacitor type and location is not risky.

Supply

The supply voltage of +8V and the ground potential for the video processor module H4VS66 is delivered from the PiP main module via connector CON3. The supply voltage and the ground is bridged to connector CON1 for supplying the third colour decoder, which is connected to CON1 and CON2.
The IC and the buffers of the PCB get a filtered supply voltage, named “+8VRGB”. The decoupling is done by the coil L504 (2.2µH) and several decoupling capacitors.
The capacitors C117 (100nF/SMD) and C118 (100µF) together with the coil remove disturbance from the external supply delivered by the PiP main PCB. The capacitor C160 (100nF/SMD) decouples the +4 V generation for pin 15 of the TDA 4780 and the buffer for the FSW output signal. The capacitor C160 (100nF/SMD) decouples the RGB output buffer of the PCB and C106 (10nF/SMD) removes disturbances from the supply pin of the TDA 4780. C106 should be located as near as possible to pin 5 of the TDA 4780.

4.3.4 Interface and Probing

The following Fig. 45 shows the placement of all major elements, the jumper for adapting the SCART socket to the two standards as well as the location of the most interesting output signals of the PCB.
Table 20 lists the relevant data of the signals on the interface connectors.

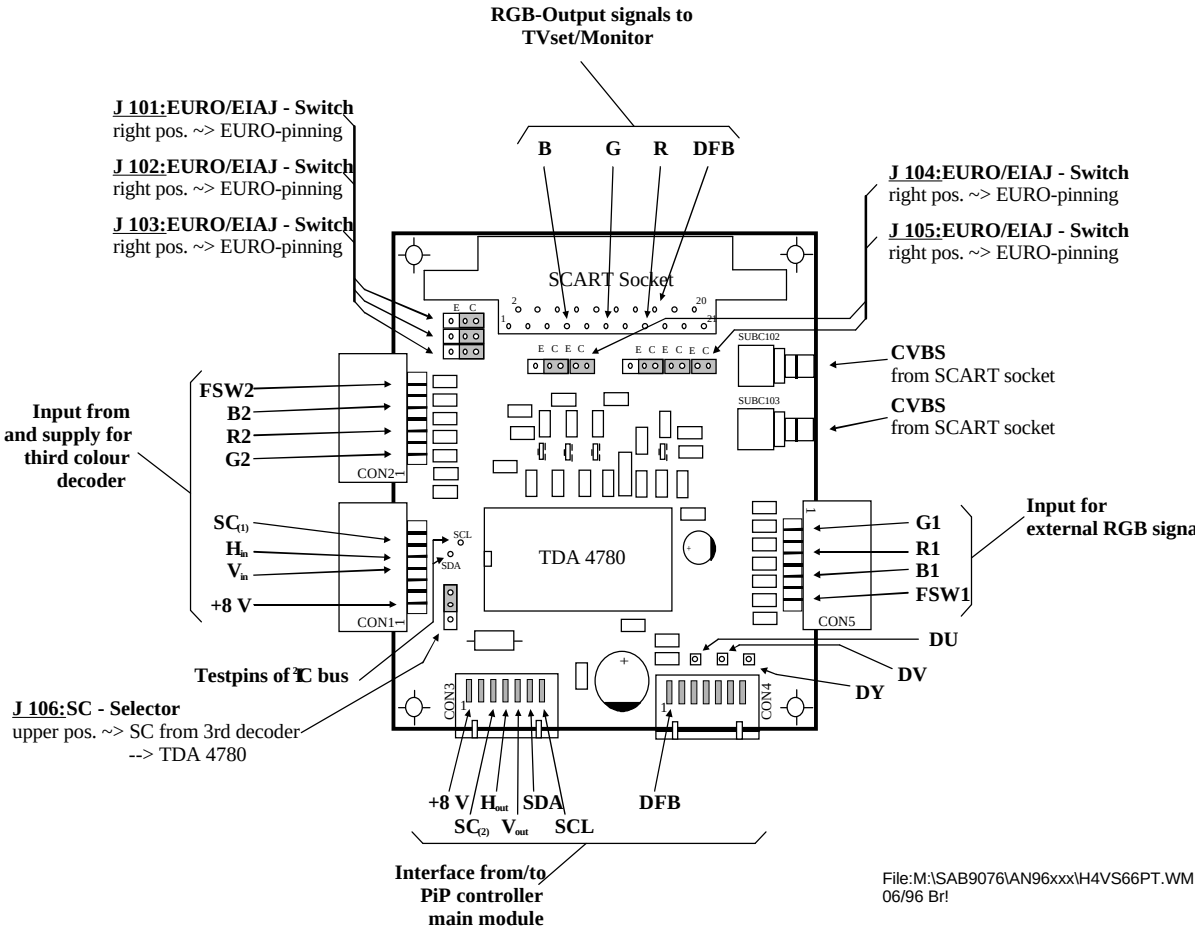


Fig.45 Relevant signals and settings of H4VS66

TABLE 20 Characteristics of Interface-signals

Cond.: PAL Standard Colour Bar Testsignal 100/0/75/0 to all three colour decoder; Supply = 8V							
Connector/Pin	**Signal-name**	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
CON1/ Pin 1	+8V						Supply Voltage for third colour decoder
CON1/Pin 4	V	5.2 Vpp	0 V	5.2V	320 µs	20 ms	
CON1/Pin 5	H	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	
CON1/Pin 6	SC(1)	4.8 Vpp	0 V	4.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 910µs	64 µs	Burst-Key-Top =4.8 V_{DC} H-Pulse-Top = 2.4 V_{DC} V-Pulse-Top = 2.4 V_{DC}
CON2/Pin 1	G2	0.7 Vpp					
CON2/Pin 3	R2	0.7 Vpp					
CON2/Pin 5	B2	0.7 Vpp					
CON2/ Pin 7	FSW2		0.4V max	0.9 V min	as required		high active, lower priority than FSW1
CON3/Pin 3	SC(2)	4.8 Vpp	0 V	4.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 910µs	64 µs	Burst-Key-Top =4.8 V_{DC} H-Pulse-Top = 2.4 V_{DC} V-Pulse-Top = 2.4 V_{DC}
CON3/Pin 4	Hout	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	
CON3/Pin 5	Vout	5.2 Vpp	0 V	5.2V	320 µs	20 ms	
CON3/Pin 6	SDA	5.0 Vpp	0 V	5.0 V			low active; clock & data appear only during data transmission
CON3/ Pin 7	SCL	5.0 Vpp	0 V	5.0 V			
CON4/Pin 1	DFB	5.0 Vpp	0 V	5.0 V	as required	as required	
CON4/Pin 3	DU [B-Y]	1.33 Vpp	490 mV	1.82 V			no-colour-Level = 1.13 V
CON4/Pin 5	DV [R-Y]	1.05 Vpp	235 mV	1.28 V			no-colour-Level = 780 mV
CON4/ Pin 7	DY	315 mVpp					Black Level = 80 mV
CON5/Pin 1	G1	0.7 Vpp					
CON5/Pin 3	R1	0.7 Vpp					
CON5/Pin 5	B1	0.7 Vpp					
CON5/ Pin 7	FSW1		0.4 V max	0.9 Vmin	as required		high active, higher priority than FSW2
SUBC102	CVBS from SCART	1 Vpp				64 µs	DC level depends on TV-set, used as signal source

TABLE 20 Characteristics of Interface-signals

Cond.: PAL Standard Colour Bar Testsignal 100/0/75/0 to all three colour decoder; Supply = 8V							
Connector/Pin	**Signal-name**	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
SUBC103	CVBS to SCART	1 Vpp				64 µs	
SCART/Pin 15	R	1 Vpp	930 mV	1.93 V	as required	as required	depending on setting of TDA 4780
SCART/Pin 11/19*	G	1 Vpp	870 mV	1.87 V	as required	as required	depending on setting of TDA 4780
SCART/Pin 7/20*	B	1 Vpp	870 mV	1.87 V	as required	as required	depending on setting of TDA 4780
SCART/Pin 16	FSW	2.24 Vpp	0 V	2.24 V	as required	as required	

4.3.5 Layout and Placement

The following figures show the layout and placement for the H4VS66 module in original size.

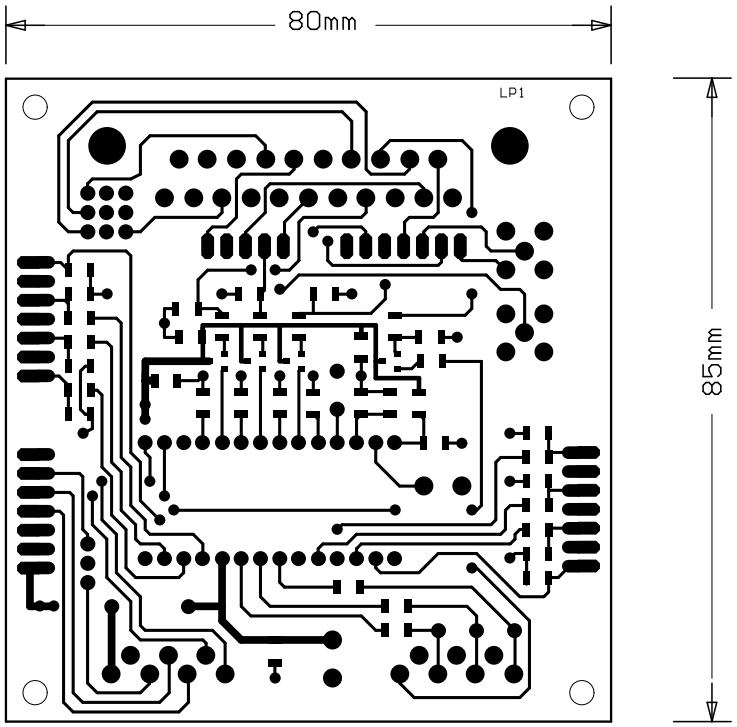


Fig.46 Layout of the H4VS66 Topside

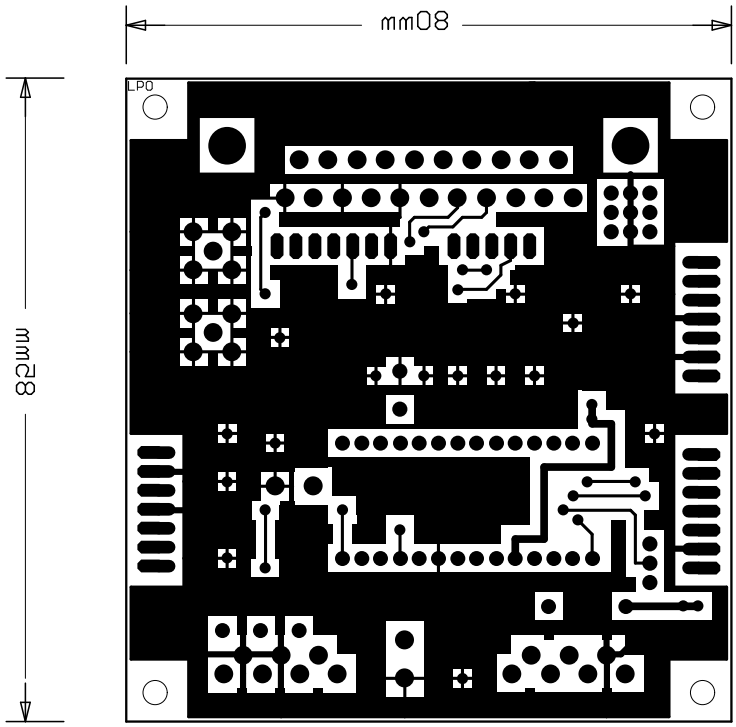


Fig.47 Layout of H4VS66 Bottomside

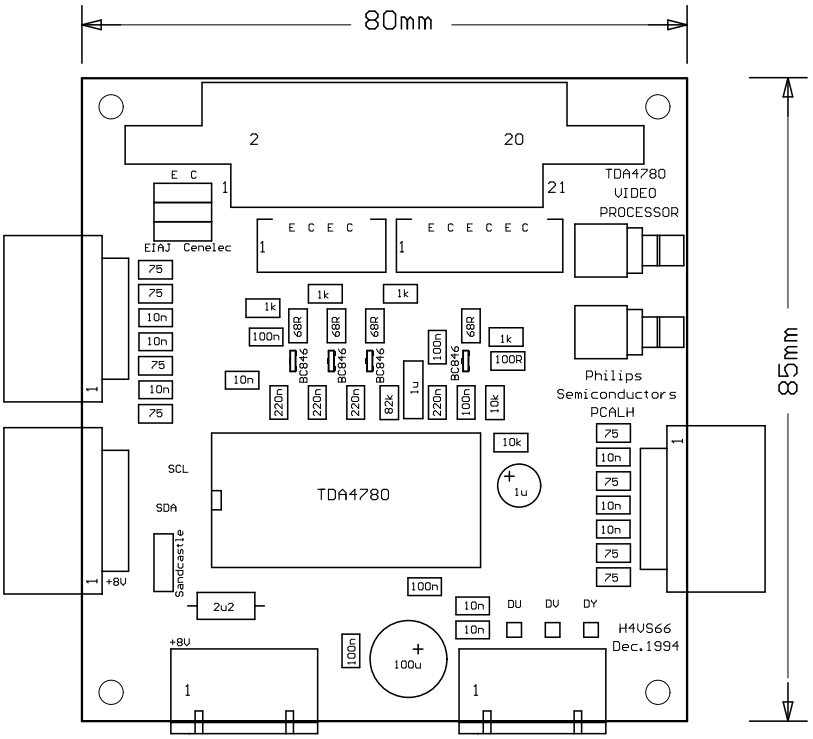


Fig.48 Placement of Topside Components

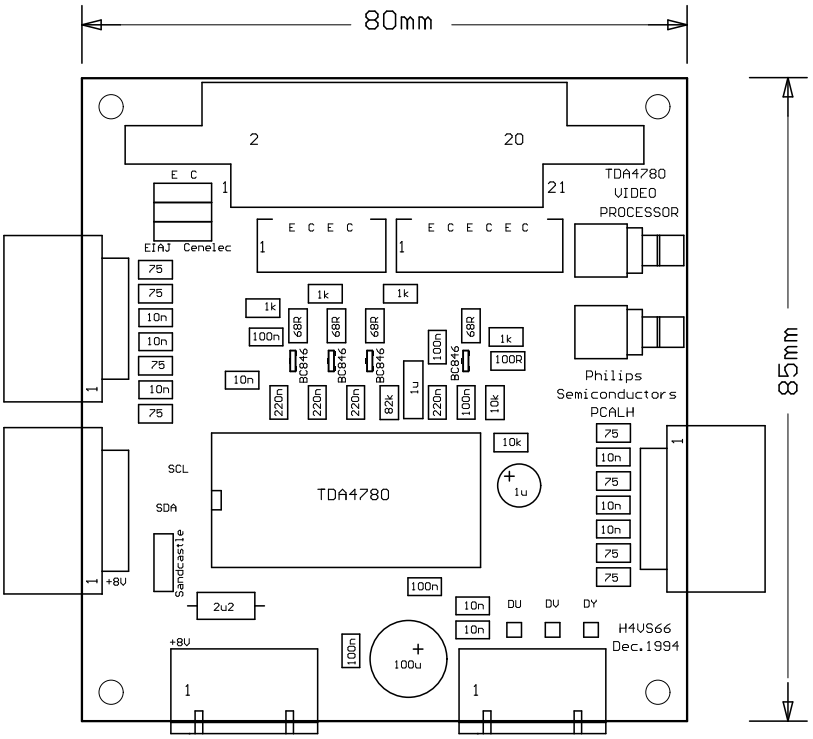


Fig.49 Values of Topside Components

4.3.6 Application hints

The video backend processor module H4VS66 is designed as a double sided PCB. The components are place on the topside only for simplifying probing, testing and evaluation. For implementation the circuitry in an environmental PCB design the components can be placed on the bottomside and a multilayer design is possible even too.
It should be taken care of the distance between the storage capacitors C 110, C111, C112 and the IC for preventing the IC inputs from disturbances. The distance should be as short as possible.

4.4 PiP Controller SAB 9076/77 on H6VS01

The PiP controller SAB 9076/77 itself is described in the Application Note AN 96026 " Application Information for Picture in Picture Controller SAB 9076 ".

4.4.1 Description of the Main module H6VS01

The main module H6VS01 is the centre of the PiP evaluation boardset. It gathers the video signals and their associated synchronisation signals from the main- and subchannel colour decoders. The PCB includes the PiP controller SAB 9076/77 with its environment and a 2MBit VideoDRAM as shadow memory. The main module feeds its output signals to the video processor module H4VS66.
The module contains the distribution of the supply voltage, the ground and the I^2C bus commands.

The blockdiagram of the main module H6VS01 is shown in Fig. 50 .

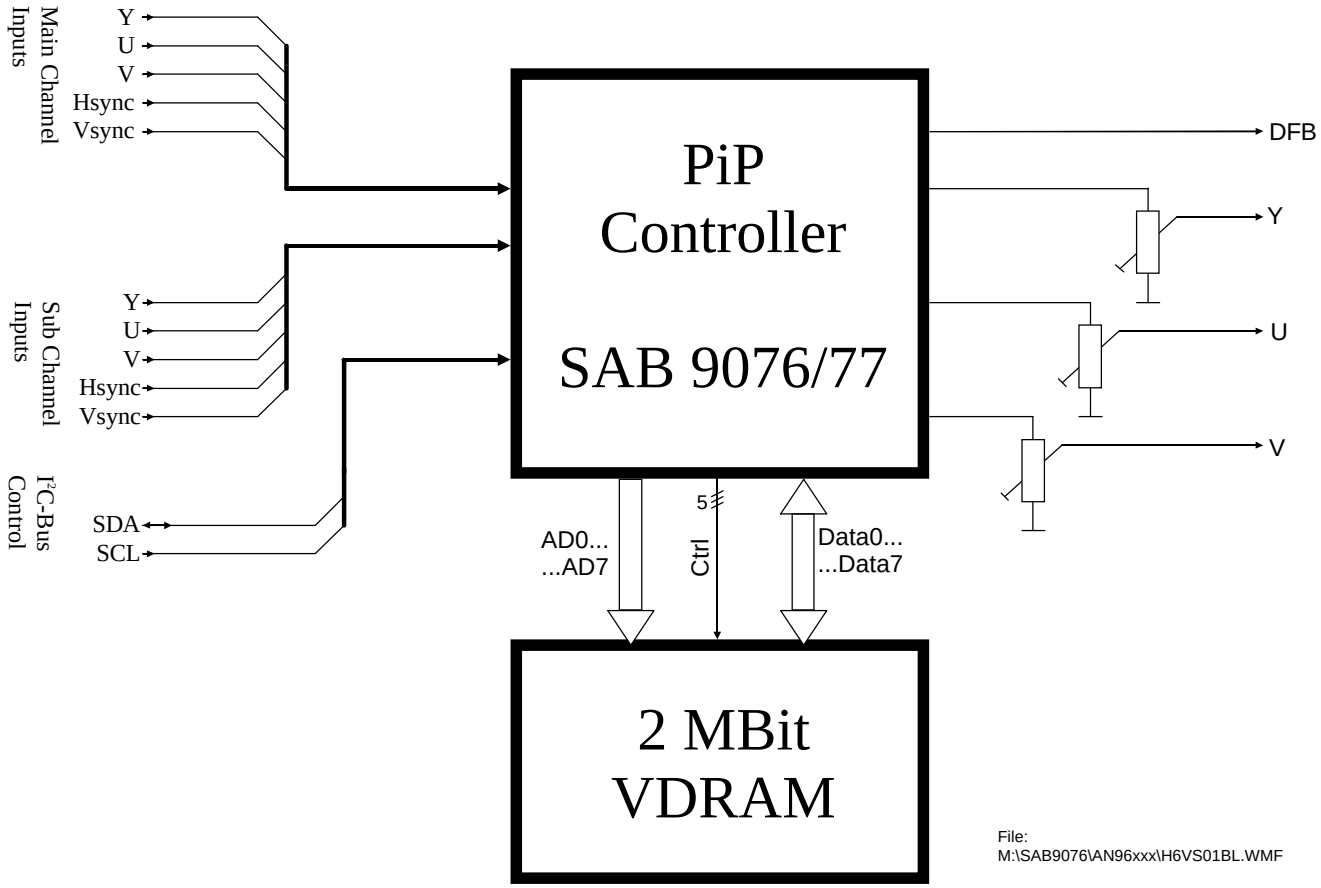


Fig.50 Blockdiagram of the main module H6VS01

The following figures show the schematics of the main module H6VS01.

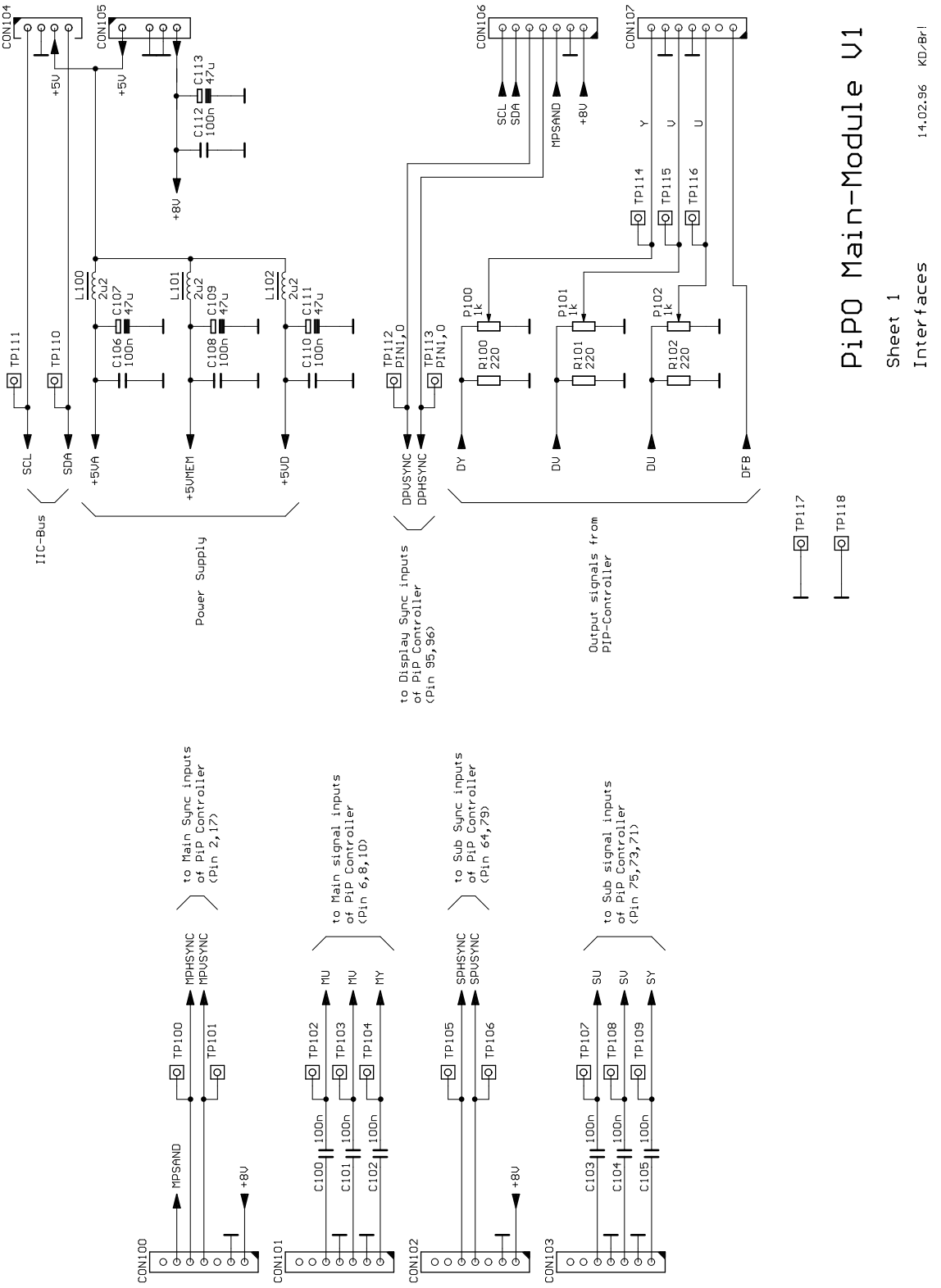


Fig.51 Interfaces of the main module H6VS01

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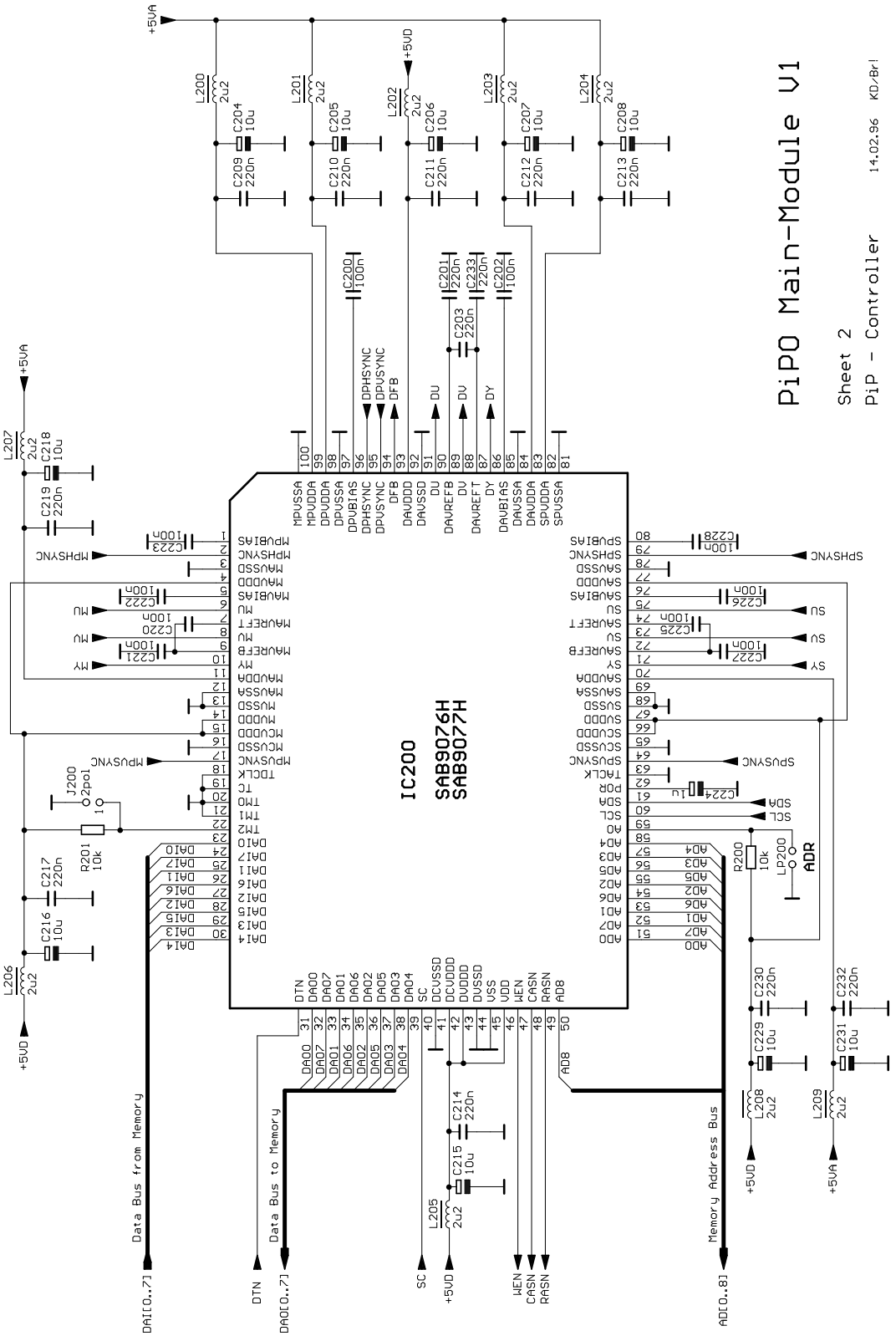

Fig.52 Application and environment of the SAB9076/77

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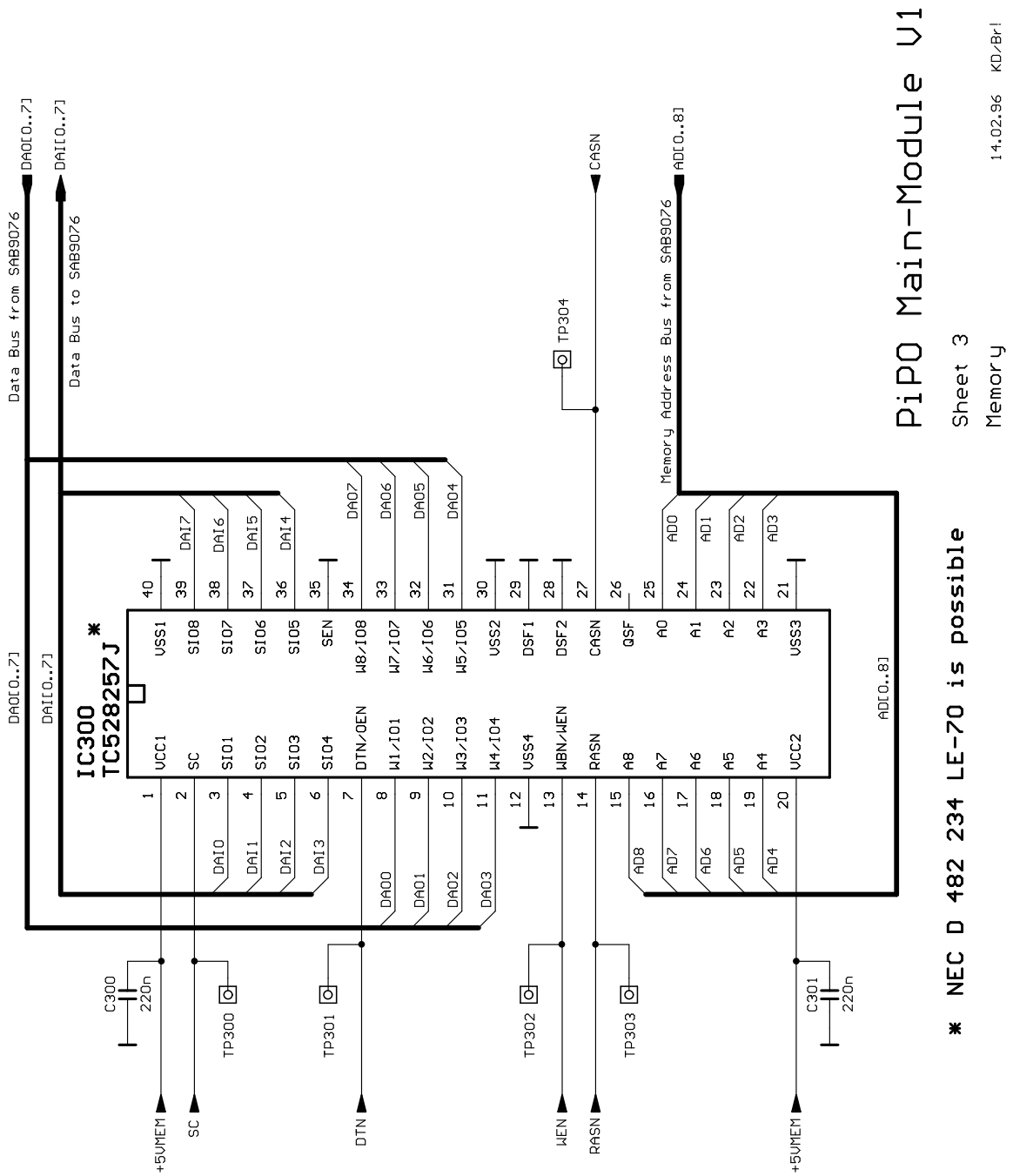

Fig.53 Application and environment of the Memory IC

General

The main module H6VS01 contains the complete application environment for the PiP controller SAB 9076/77 and its associated shadow memory. The PCB provides standardized input interfaces to the main channel and sub channel colour decoder modules H4VS65 (NTSC) or H5VS48 (multistandard). The output signals of the PiP controller are adjustable in gain and provided together with the associated fast blanking signal for the backend video processor at the output interface.
The PCB contains the power distribution for all connected colour decoders and for the video backend processor as well as the I^2C link to the video the backend processor.

Inputs

The YUV signals of the main channel colour decoder with their associated H- and V-synchronization signals are connected to the main module at the input connectors CON100 and CON101. The YUV signals are AC coupled with 100nF capacitors each to the pins 10 (MY), 6 (MU) and 8 (MV) of the PiP controller. Behind the coupling/ clamping capacitors the input signals can be probed at the testpins TP102 [MU], TP103 [MV] and TP104 [MY]. This offers the possibility to check the clamping level of the PiP controller inputs. The inputs are not terminated.

The main channel synchronization signals MPHSYNC and MPVSYNC are directly coupled to the input pins 2 [MPHSYNC] and 17 [MPVSYNC] of the PiP controller. For testing and equipment synchronization purposes these signals are available at the testpins TP100 [MH] and TP101 [MV].

The colour decoder modules H4VS65 (NTSC) and H5VS48 (multistandard) generate a sandcastle signal and provide it as an output signal on the interface to the main module. For the main channel this sandcastle signal is picked up and bridged to the interface of the video backend processor. As described on page 67, a selection out of two sandcastle signals can be made on the video processor module H4VS66, to sychronize the TDA 4780.

The connection of the sub channel colour decoder module to the main module is similar to the description above. The YUV signals of the sub channel colour decoder with their associated H- and V- synchronization signals are connected to the main module at the input connectors CON102 and CON103. The YUV signals are AC coupled with 100nF capacitors each to the pins 71 (SY), 75(SU) and 73(SV) of the PiP controller. Behind the coupling/ clamping capacitors the input signals can be probed at the testpins TP107 [SU], TP108 [SV] and TP109 [SY]. This offers the possibility to check the clamping level of the PiP controller inputs. The inputs are not terminated.

The sub channel synchronization signals SPHSYNC and SPVSYNC are directly coupled to the input pins 79 [SPHSYNC] and 64[SPVSYNC] of the PiP controller. For testing and equipment synchronization purposes these signals are available at the testpins TP105 [SH] and TP106 [SV].

The sandcastle signal generated by the sub channel colour decoder module is not used on the main module.

The I^2C bus signals SDA and SCL are connected to the PCB by the connector CON104. The signals are fed to the PiP controller as well to the backend video processor TDA 4780, connected to the main module by connector CON106 on pins 6,7. The I2C bus signals can be probed at the testpins TP110 [SDA] and TP111 [SCL]. The bus is not terminated by pull-up resistors.

The PiP controller receives the H- and V pulses to synchronize it's display part from the third colour decoder via the video processor module H4VS66. The synchronization signals are available at connector CON106 on pin 4 [DPHSYNC] and pin 5 [DPVSYNC]. The signals are directly connected to the PiP controller. They can be probed at the testpins TP113 [DH] and TP112 [DV].

Outputs

The output signals of the main module are available to the connectors CON106 and CON107. Connector CON106 carries the synchronization signals and CON107 the YUV signals and the associated fast blanking signal DFB.
The output pins of the PiP controller have to be loaded by a pull down resistor of 220Ω. To adjust the amplitude of the YUV signals, a potentiometer is connected in parallel to the load resistor for each of the YUV signals. The gain corrected YUV signals can be probed at the testpins TP114 [Y], TP115 [V] and TP116 [U] and they are connected to the pins 7 [Y], 5 [V] and 3 [U] of connector CON107. The pins 4 and 6 of CON107 are grounded for shielding purposes.
The fast blanking pulse [DFB], provided by the PiP controller, is directly fed to pin 1 of connector CON107. For this signals is no testpin available, because a test equipment can be synchronized with the DPHSYNC or DPVSYNC signals as well. To avoid crosstalk from the fast blanking signal to the YUV signals a shielding between these signals should be provided.

Connector CON106 carries the output signals SDA (pin 6), SCL (pin 7) and MPSAND (pin 3). SDA and SCL are the I^2C bus signals to control the backend video processor TDA 4780. They can be probed at the testpins TP 110 [SDA] and TP111 [SCL].
MPSAND is the bridged sandcastle signal, generated by the main channel colour decoder module. This signal is intended to be selected for synchronization of the video processor TDA 4780 by the jumper J106, located on the video processor modul H4VS66.

IC controls

The memory IC300 (TC528 257J from Toshiba or D 482 234 LE-70 form NEC) doesn't need any adjustments, controls and initializations.
The PiP controller SAB 9076/77 has to be initialized by I^2C bus. All further controls and adjustments have to be made by the I^2C bus. Two major items have to be set by hardware.

1. I2C bus address
2. Input level selection

The I^2C bus address of the PiP controller can be set between the addresses 2C and 2E by applying a DC voltage of 0V or 5V to pin 59 of the IC.

TABLE 21 Setting of I^2C bus address for SAB 9076/77

I^2C bus address	Voltage at pin 59	Solder pad LP200	Remark
2C	0V	short	default setting
2E	5V	open	

Pin 59 of the PiP controller is connected via a pull-up resistor of 10kΩ to the digital supply voltage +5VD. The default is setting the IC to the address 2C by grounding pin 59 with a short on the solder pad LP200.

The pins 18 to 22 of the PiP controller are testpins for the automatic production tester. They are unimportant for normal operation conditions, except pin 22 (TM2).
The multistandard device SAB 9077 provides the capability to adapt the level range of the YUV inputs of the main- and the sub acquisition channel to several input signal levels. The NTSC colour decoder module with the TDA 8315T delivers the YUV signals with an amplitude of 1.5 Vpp each. In contrast to that, the multistandard colour decoder TDA 8310A provides the YUV signals with a nominal amplitude of 1.0Vpp for Y, 1.05Vpp for V and 1.33Vpp for U. To get the same signal level as the NTSC colour decoder module, three amplifiers are incorporated on the multistandard colour decoder module H5VS48. This has historical causes, because the multistandard colour decoder module H5VS48 was developed before the level adaption was implemented in the SAB 9077.

Using the latest version of the SAB 9077 makes the amplifier on the H5VS48 unnecessary.
The input signal level adaption is set by the DC voltage applied to pin22 (TM2) of the PiP controller SAB 9077. The pin is connected to the digital supply voltage +5VD via a pull-up resistor of 10kΩ. The jumper J200 sets the pin to ground if shorted.

TABLE 22 Input level adaption of SAB 9077

Voltage at pin 22 (TM2)	Nominal input level range		Level range adapted to:	Colour standard	Setting of jumper J200
0V (Vss)	Y	1.0Vpp	TDA 8310A	Multistandard	short
	U	1.33Vpp			
	V	1.05Vpp			
5V (Vdd)	Y	1.5Vpp	TDA 8315T	NTSC only	open
	U	1.5Vpp			
	V	1.5Vpp			

Remark:
If the NTSC only version of the PiP controller (SAB 9076) is used, the DC voltage at pin 22 has no influence of the IC. The pin is internally connected to Vdd and hence the inputs are prepared for the signal levels of the NTSC colour decoder TDA 8315T (1.5Vpp for Y,U and V).

Supply

The main module H6VS01 contains the power supply and ground distribution for all components of the PiP boardset.
The boardset needs two supply voltages, 8V for the colour decoder modules and the video processor TDA 4780 and 5V for the PiP controller, the memory and the I^2C bus. Supply and ground are connected to the boardset by the connector CON105.

The +8V supply is fed to the boardset at pin 4 of connector CON105, decoupled by the capacitors C112 (100nF) and C113 (47 µF) and then directly distributed to CON100, pin 1 for the main channel colour decoder module, to CON102, pin 1 for the sub channel colour decoder module and to CON106, pin1 for the video processor module and the attached third colour decoder module.

The +5V supply is connected to the boardset at pin 1 of connector CON105. The supply is directly bridged to pin 3 of the I^2C bus connector CON104. This is indended for bus masters, which need a external supply.
For the internal use on the main module, the +5V supply is splitted up into three pathes:

1) +5VA for supplying the analog parts of the PiP controller
2) +5VD for supplying the digital parts of the PiP controller
3) +5VMEM for supplying the memory IC separately from the PiP controller.

Each of the supply pathes has a decoupling network, consisting out of a coil of 2.2µH in series with two capacitors of 100nF and 47µF in parallel.

The supply for the memory is connected to the pins 1 and 20 of the IC. Each memory supply pin has its own decoupling capacitor connected to the associated ground pin of the IC.

The supply pathes for +5VA and +5VD are splitted up into sub pathes, each path with an own decoupling network. The decoupling network of the sub pathes consist of a coil of 2.2µH and in series an combination of an 220nF SMD chip capacitor and a 10µF electrolytic capacitor in parallel. These decoupling networks are located as near as possible to the PiP controller supply pins. The power distribution is designed very extensively,

because the several supply pins of the PiP controller generate a lot of clock noise, which should be kept close to the IC itself. Overmore, the several supply pins should be separated as much as possible.

The ground connection of the IC's, the decoupling networks and all other components is made by a common ground plane on the top side of the PCB. Our experience has shown, that a ground separation between analog and digital ground is unfavourable for a good clock noise suppression.

Two testpins on the opposite corners of the PCB (TP117, TP118) are included for grounding the test- and measurement equipment. The several supply voltages have no testpins.

Further application hints

As mentioned before, the decoupling networks of the +5VA- and +5VD sub pathes have to be located as near as possible to the supply pins of the IC to keep the clock noise next to the IC and to avoid long supply lines acting as antennas.
The main module H6VS01 is designed following the idea to keep all supply lines and synchronization lines on the top side of the PCB together with the common ground plane. The ground plane acts as shielding between sensitive lines, to suppress crosstalk. Corresponding to this idea, all signal lines are located on the bottom side of the PCB. Especially the layout for the YUV input signal lines for both the main and the sub channel should be made very carefully to avoid crosstalk from noisy lines into the AD-converter inputs.
The placement of the PiP controller IC and the memory IC should be made as recommended on the main module. The pinning of the PiP controller concerning the connection of the memory IC is chosen to design a single sided crossfree bus layout.

4.4.2 Interface and Probing

The following Fig. 54 shows the placement of all major elements, the jumper for selecting the sandcastle signal to synchronize the video processor TDA 4780, the solder pad for determing the I^2C bus address of the PiP controller as well as the location of the most interesting output signals of the PCB.
Table 23 lists the relevant data of the signals on the interface connectors.

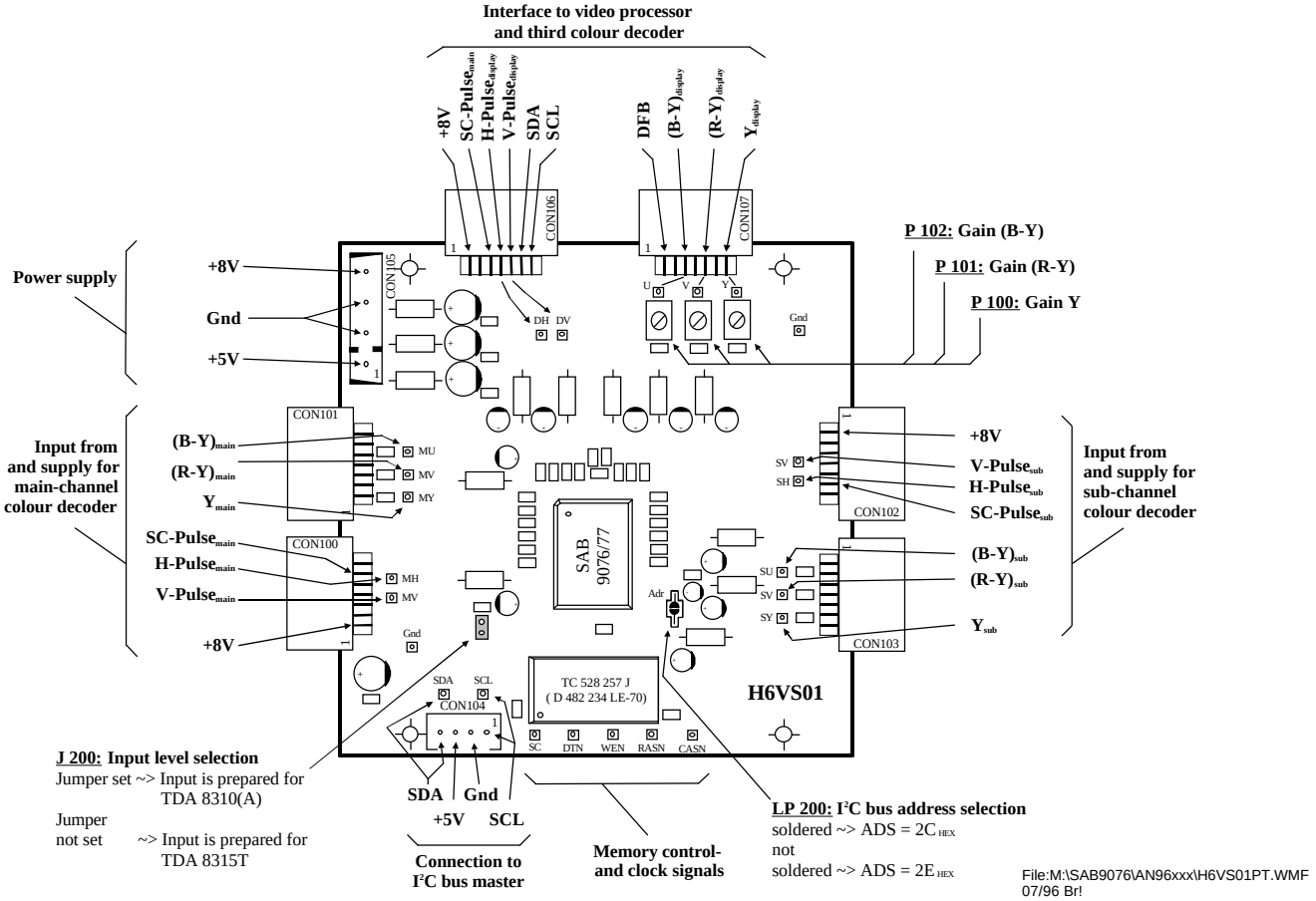

Fig.54 Relevant signals and settings of H6VS01

TABLE 23 Characteristics of Interface-signals

Cond.: PAL Standard Colour Bar Testsignal 100/0/75/0 to all three colour decoder; Supply = 8V							
Connector/Pin	**Signal-name**	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
CON100/Pin 1	+8V						Supply Voltage for main channel colour decoder
CON100/Pin 4	MPVSYNC	5.2 Vpp	0 V	5.2V	320 µs	20 ms	
CON100/Pin 5	MPHSYNC	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	
CON100/Pin 6	MPSAND	4.8 Vpp	0 V	4.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 910µs	64 µs	Burst-Key-Top =4.8 V_{DC} H-Pulse-Top = 2.4 V_{DC} V-Pulse-Top = 2.4 V_{DC}
CON101/Pin 1	MY	2.0 Vpp	0.4 V Sync Bottom	2.4 V White peak		64 µs	Black-Level = 0.9V_{DC} Luminance = 1.5 Vpp
CON101/Pin 3	MV	1.5 Vpp	0.75 V	2.25 V		64 µs	no-colour-Level = 1.5V_{DC}
CON101/Pin 5	MU	1.5 Vpp	0.5 V	2.0 V		64 µs	no-colour-Level = 1.25V_{DC}
CON102/Pin 1	+8V						Supply Voltage for sub channel colour decoder
CON102/Pin 4	SPVSYNC	5.2 Vpp	0 V	5.2V	320 µs	20 ms	
CON102/Pin 5	SPHSYNC	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	
CON103/Pin 1	SY	2.0 Vpp	0.4 V Sync Bottom	2.4 V White peak		64 µs	Black-Level = 0.9V_{DC} Luminance = 1.5 Vpp
CON103/Pin 3	SV	1.5 Vpp	0.75 V	2.25 V		64 µs	no-colour-Level = 1.5V_{DC}
CON103/Pin 5	SU	1.5 Vpp	0.5 V	2.0 V		64 µs	no-colour-Level = 1.25V_{DC}
CON104/Pin 1	SCL	5.0 Vpp	0 V	5.0 V			low active; clock appears only during data transmission
CON104/Pin 2	Gnd						
CON104/Pin 3	+5V						supply output for bus master
CON104/Pin 4	SDA	5.0 Vpp	0 V	5.0 V			low active; data appears only during data transmission
CON105/Pin 1	+5V						+5V supply for complete boardset & I^2C bus master
CON105/Pin 2	Gnd						
CON105/Pin 3	Gnd						

TABLE 23 Characteristics of Interface-signals

Cond.: PAL Standard Colour Bar Testsignal 100/0/75/0 to all three colour decoder; Supply = 8V							
Connector/Pin	**Signal-name**	**Amplitude**	**Low Level**	**High Level**	**Pulse-width**	**Signal-period**	**Remark**
CON105/Pin 4	+8V						+8V supply for all colour decoder & video processor
CON106/Pin 1	+8V						+8V supply for video processor module H4VS66 and the third colour decoder
CON106/Pin 3	MPSAND	4.8 Vpp	0 V	4.8 V	$tw_{(BK)}$ = 3.4 µs $tw_{(H)}$ = 8.8 µs $tw_{(V)}$ = 910µs	64 µs	Burst-Key-Top =4.8 V_{DC} H-Pulse-Top = 2.4 V_{DC} V-Pulse-Top = 2.4 V_{DC}
CON106/Pin 4	DPHSYNC	5.0 Vpp	0 V	5.0 V	5.4 µs	64 µs	
CON106/Pin 5	DPVSYNC	5.2 Vpp	0 V	5.2V	320 µs	20 ms	
CON106/Pin 6	SDA	5.0 Vpp	0 V	5.0 V			low active; data appears only during data transmission
CON106/Pin 7	SCL	5.0 Vpp	0 V	5.0 V			low active; clock appears only during data transmission
CON107/Pin 1	DFB	5.0 Vpp	0 V	5.0 V	as required	as required	
CON107/Pin 3	DU [B-Y]	1.33 Vpp	490 mV	1.82 V			no-colour-Level = 1.13 V
CON107/Pin 5	DV [R-Y]	1.05 Vpp	235 mV	1.28 V			no-colour-Level = 780 mV
CON107/Pin 7	DY	315 mVpp					Black Level = 80 mV

4.4.3 Layout and Placement

The following figures show the layout and placement for the H6VS01 module in original size.

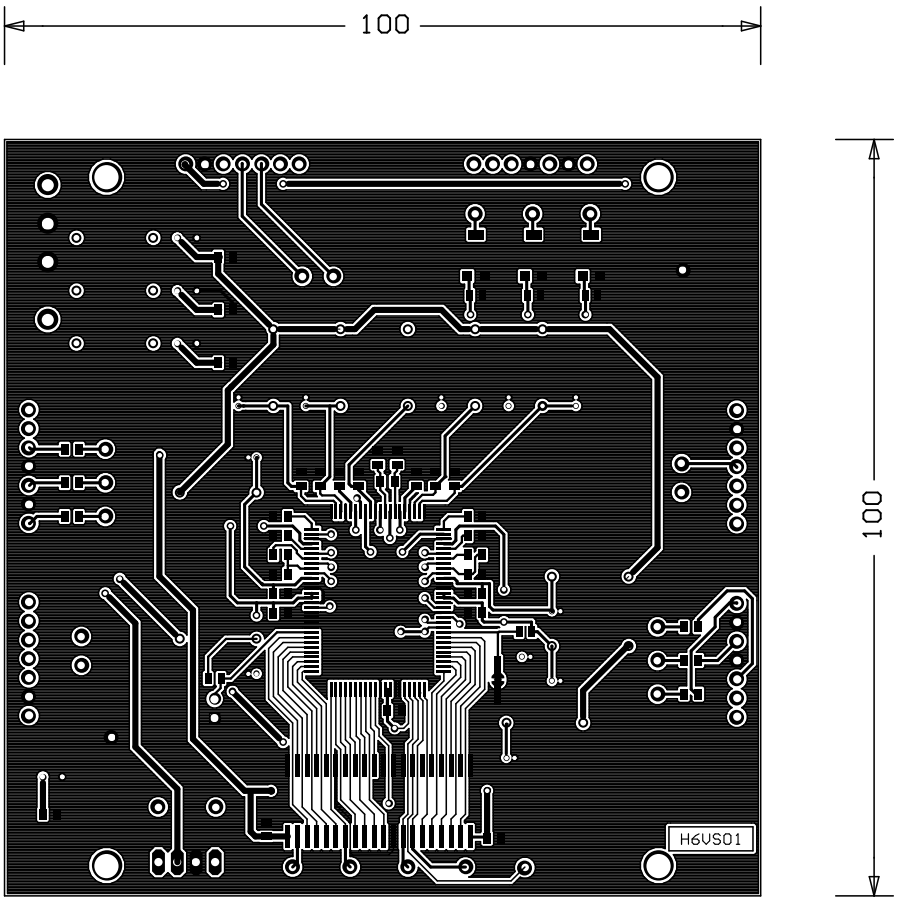

Fig.55 Layout of the H6VS01 Topside

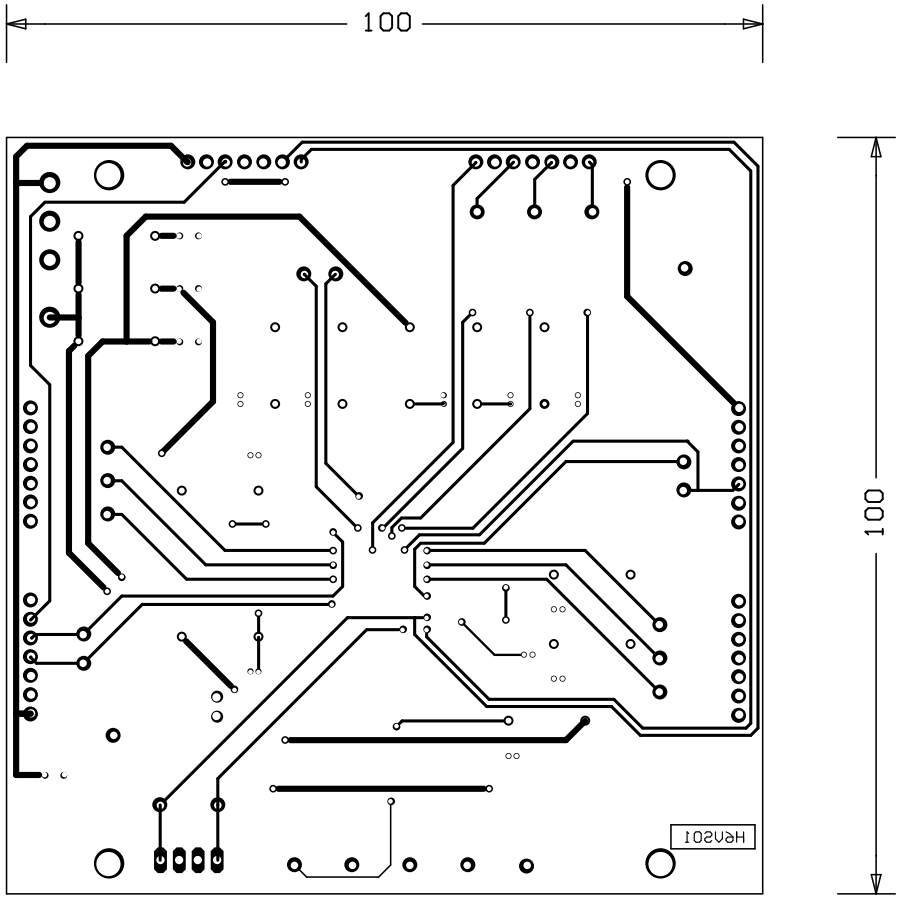

Fig.56 Layout of the H6VS01 Bottomside

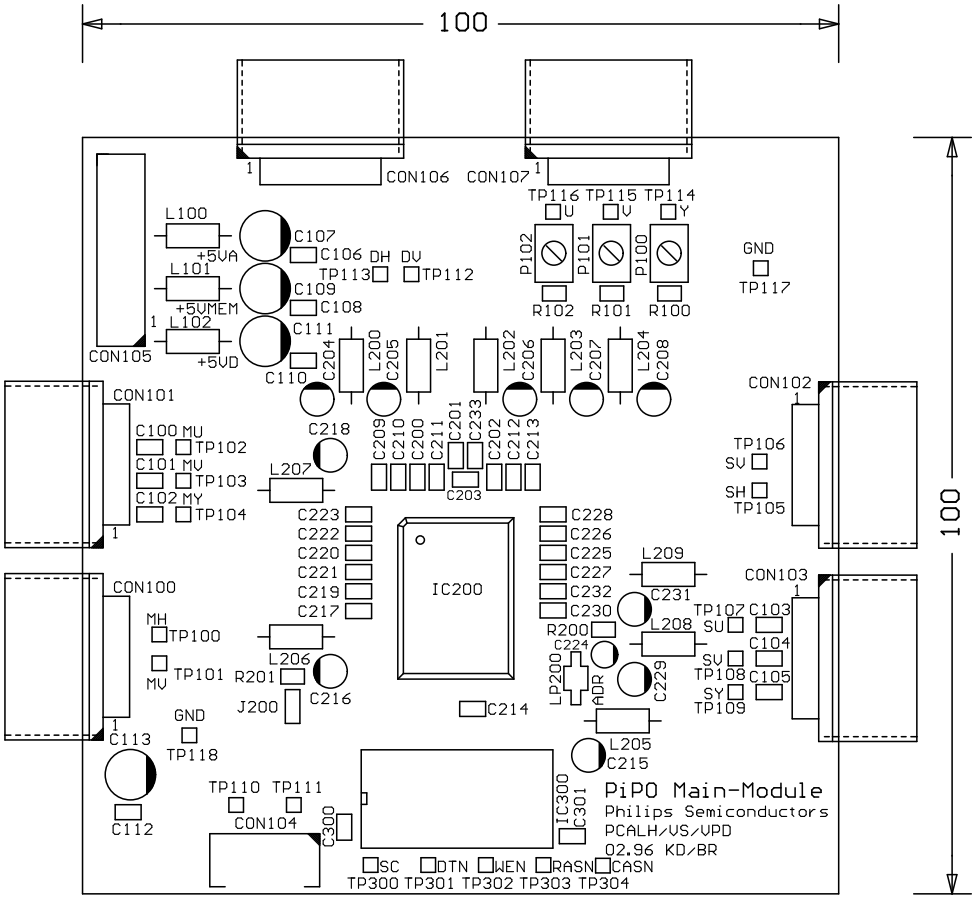

Fig.57 Placement of Topside - Components

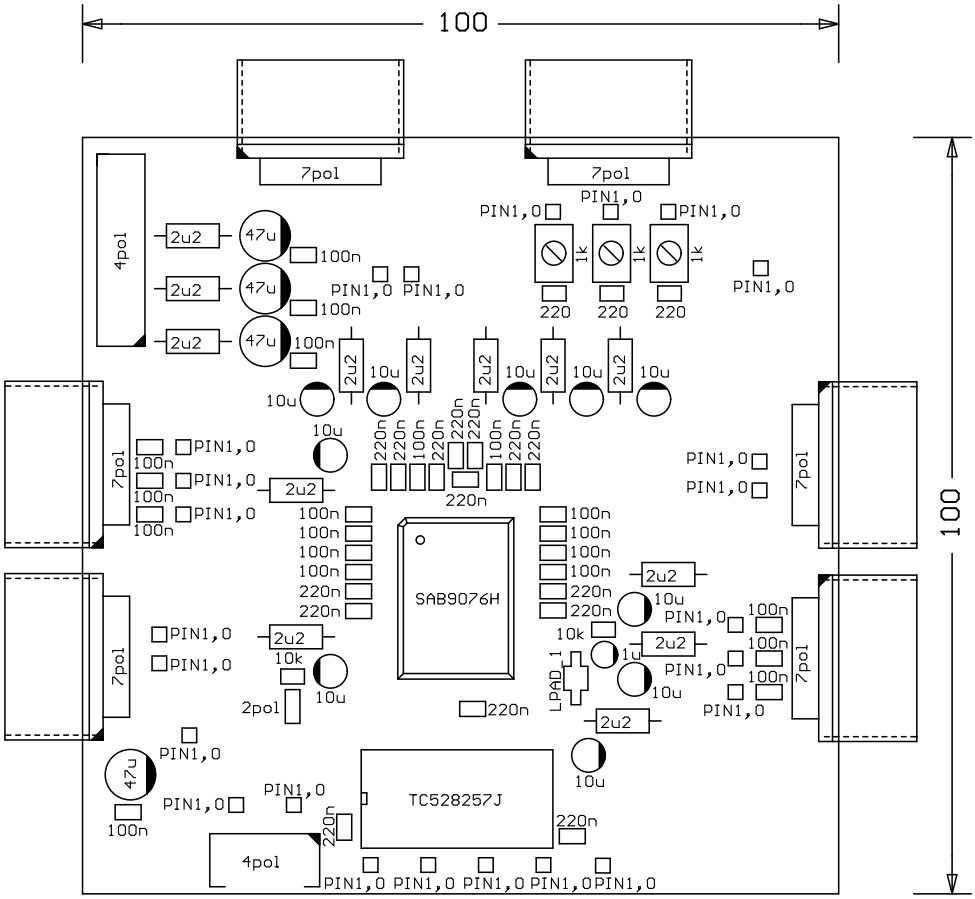

Fig.58 Values of Topside - Components

5. Application hints

All application hints are given in the specific chapters, concerning to the modules.

6. References

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7. Notes